

**Silicon Valley Expert Witness Group, Inc.
Consultant Curriculum Vitae**

R. Jacob (Jake) Baker, Ph.D., P.E.

Expertise

- CMOS Circuit Design
 - Analog Integrated Circuits
 - Mixed-Signal Design
 - Phase- and Delay-Locked Loops
 - Power MOSFET Circuit Design
 - DRAM, Flash, Resistive Memory
 - Analog-to-Digital, Digital-to-Analog Conversion
 - Delta-Sigma Techniques
 - Power Electronics
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Employment History

- From: 2000 **Boise State University**
To: Present Boise, ID
Position *2003-Present: Professor of Electrical & Computer Engineering*
 2004-2007: Department Chair
 2000-2003: Associate Professor
- Research focuses on analog and mixed-signal integrated circuit design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects funded by EPA, DARPA, NASA and the Air Force Research Lab.
 - Led the department in graduate curriculum and program development (Masters in 2000 and PhD in 2006) and an ABET accreditation visit in 2005.
 - Worked with companies, both established and start-ups (and both in and outside Idaho), to provide technical expertise and to identify employment opportunities for students.
 - Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Cooperated with College of Engineering faculty on joint research projects.
 - Taught courses in circuits, analog IC design, digital VLSI, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

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From: 1994 **Micron Technology**
To: 2008
Position: *Affiliate Faculty (Senior Designer)*
Designed CMOS circuits for DRAMs including DLLs (design is currently used in Micron's DDR memory), PLLs for embedded graphics chips, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies). Worked on a joint research project between Micron and HP labs in magnetic memory. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing.

From: 1993 **University of Idaho**
To: 2000 ID
Position *1998-2000: Associate Professor of Electrical Engineering*
 1993-1998: Assistant Professor of Electrical Engineering
Helped prepare (in 1999) the ABET 2000 accreditation report for Electrical and Computer Engineering visit (fall 2000).

From: 1991 **University of Nevada**
To: 1993 Reno, NV
Position *Lecturer, Department of Electrical Engineering*
 Taught courses in communication systems, electronics, and materials.

From: 1985 **E.G.&G. Energy Measurements Inc.**
To: 1993 NV
Position: *Senior Electronics Design Engineer*
Responsible for the design of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Sole-engineer responsible for the design of over 30 electronic and electro-optic instruments. This position provided considerable fundamental grounding in electrical engineering. Exposed to and participated in everything from PC board design to the design of cable equalizers. Gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuits, GaAs (high speed logic and HBTs), microwave techniques, etc.

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Consulting History

- From: 2009 **Sun Microsystems, Inc. (VLSI Research Group)**
To: Present Mountain View, CA
Duties: Provided consulting on memory circuit design and proximity connection (PxC) interfaces to DRAMs and SRAMs
- From: 2008 **Nascentric**
To: 2008 Austin, TX
Duties: Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.
- From: Summer **Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc.**
To: 1998
Duties: Design PLLs and DLLs for custom ASICs and a graphics controller chip.
- From: 1997 **Tower Semiconductor**
To: 1998 Haifa, Israel
Duties: Designed CMOS integrated circuit cells for various modem chips.
- From: Summers **Micron Display Inc.**
To: 1994 &
1995
Duties: Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wristwatch size color television.
- From: 09/1993 **Lawrence Berkeley Laboratory**
To: 10/1993
Duties: Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns risetime and 8 ns falltime for driving Helmholtz coils.
- From: Summer **Lawrence Livermore National Laboratory, Nova Laser Program**
To: 1993
Duties: Performed research in picosecond instrumentation, including time-domain design for impulse radar and imaging.

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From: Summer **Reynolds Electrical Engineering Company**
To: 1995 Las Vegas, NV
Duties: Gained hands on experience in primary and secondary power system design and installation and trouble shooting electric motors on mining equipment.

Litigation Support Experience

2009-present Exclusive Consultant for Silicon Valley Expert Witness Group
(<http://www.svewg.com/>)

1997-2008 Provided depositions and expert testimony in areas ranging from delay-locked loop design to fire alarm wiring reliability. Helped the Federal Trade Commission and International Trade Commission by providing explanations of how Rambus technology works and how it relates to mainstream DRAM interfaces for synchronous DRAMS.

Patents

<u>Patent Number</u>	<u>Date Issued</u>	<u>Title</u>
7,538,702	05/26/2009	Quantizing circuits with variable parameters
7,528,877	05/05/2009	Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors
7,515,188	04/07/2009	Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors
7,495,964	02/24/2009	Method and apparatus for sensing flash memory using delta-sigma modulation
7,489,575	02/10/2009	Noise resistant small signal sensing circuit for a memory device
7,456,885	11/25/2008	Per column one-bit ADC for image sensors
7,449,953	11/11/2008	Input buffer design using common-mode feedback
7,421,607	09/02/2008	Method and apparatus for providing symmetrical output data for a double data rate DRAM
7,372,717	05/13/2008	Methods for resistive memory element sensing using averaging
7,366,021	04/29/2008	Method and apparatus for sensing flash memory using delta-sigma modulation
7,366,003	04/29/2008	Method of operating a complementary bit resistance memory sensor and method of operation
7,330,390	02/12/2008	Noise resistant small signal sensing circuit for a memory device

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<u>Patent Number</u>	<u>Date Issued</u>	<u>Title</u>
7,319,620	01/15/2008	Input and output buffers having symmetrical operating characteristics and immunity from voltage variations
7,310,018	12/18/2007	Method and apparatus providing input buffer design using common-mode feedback
7,286,428	10/23/2007	Offset compensated sensing for a magnetic random access memory
7,271,635	09/18/2007	Method and apparatus for reducing duty cycle distortion of an output signal
7,268,603	09/11/2007	Method and apparatus for reducing duty cycle distortion of an output signal
7,251,177	07/31/2007	Skewed sense AMP for variable resistance memory sensing
7,242,603	07/10/2007	Method of operating a complementary bit resistance memory sensor
7,237,136	06/26/2007	Method and apparatus for providing symmetrical output data for a double data rate DRAM
7,224,632	05/29/2007	Rewrite prevention in a variable resistance memory
7,151,689	12/19/2006	Integrated charge sensing scheme for resistive memories
7,133,307	11/07/2006	Adjusting the frequency of an oscillator for use in a resistive sense amp
7,123,525	10/17/2006	Phase detector for all-digital phase locked and delay locked loops
7,109,545	09/19/2006	Integrated circuit memory with offset capacitor
7,102,932	09/05/2006	Input and output buffers having symmetrical operating characteristics and immunity from voltage variations
7,095,667	08/22/2006	Noise resistant small signal sensing circuit for a memory device
7,082,045	07/25/2006	Offset compensated sensing for a magnetic random access memory
7,009,901	03/07/2006	System and method for sensing data stored in a resistive memory element using one bit of a digital count
7,002,833	02/21/2006	Complementary bit resistance memory sensor and method of operation
6,987,701	01/17/2006	Phase detector for all-digital phase locked and delay locked loops
6,985,375	01/10/2006	Adjusting the frequency of an oscillator for use in a resistive sense amp
6,954,392	10/11/2005	Method for reducing power consumption when sensing a resistive memory
6,954,391	10/11/2005	Noise resistant small signal sensing circuit for a memory device
6,954,390	10/11/2005	Noise resistant small signal sensing circuit for a memory device

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<u>Patent Number</u>	<u>Date Issued</u>	<u>Title</u>
6,950,487	09/27/2005	Phase splitter using digital delay locked loops
6,930,442	08/16/2005	Method and apparatus for measuring current as in sensing a memory cell
6,917,534	07/12/2005	Offset compensated sensing for a magnetic random access memory
6,914,454	07/05/2005	High speed low power input buffer
6,913,966	07/05/2005	Method for stabilizing or offsetting voltage in an integrated circuit
6,829,188	07/05/2005	Dual loop sensing scheme for resistive memory elements
6,909,656	06/21/2005	PCRAM rewrite prevention
6,901,020	05/31/2005	“Integrated charge sensing scheme for resistive memories
6,888,771	05/03/2005	Skewed sense AMP for variable resistance memory sensing
6,885,580	04/26/2005	Method for reducing power consumption when sensing a resistive memory
6,882,578	04/19/2005	PCRAM rewrite prevention
6,870,784	03/22/2005	Integrated charge sensing scheme for resistive memories
6,859,383	02/22/2005	Sensing method and apparatus for a resistive memory device
6,856,564	02/15/2005	Noise resistant small signal sensing circuit for a memory device
6,856,532	02/15/2005	Offset compensated sensing for a magnetic random access memory
6,829,188	12/07/2004	Dual loop sensing scheme for resistive memory elements
6,826,102	11/30/2004	Noise resistant small signal sensing circuit for a memory device
6,822,892	11/23/2004	Resistive memory element sensing using averaging
6,813,208	11/02/2004	System and method for sensing data stored in a resistive memory element using one bit of a digital count
6,809,981	10/26/2004	Wordline driven method for sensing data in a resistive memory array
6,798,705	09/28/2004	Noise resistant small signal sensing circuit for a memory device
6,795,359	09/21/2004	Methods and apparatus for measuring current as in sensing a memory cell
6,791,859	09/14/2004	Complementary bit PCRAM sense amplifier and method of operation
6,785,156	08/31/2004	Method and apparatus for sensing resistance values of memory cells
6,779,126	08/17/2004	Phase detector for all-digital phase locked and delay locked loops
6,774,690	08/10/2004	Digital dual-loop DLL design using coarse and fine loops
6,771,249	08/03/2004	Producing walking one pattern in shift register
6,741,490	05/25/2004	Sensing method and apparatus for resistance memory device

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<u>Patent Number</u>	<u>Date Issued</u>	<u>Title</u>
6,704,881	03/09/2004	Method and apparatus for providing symmetrical output data for a double data rate DRAM
6,687,179	02/03/2004	Method and system for writing data in an MRAM memory device
6,683,475	01/27/2004	High speed digital signal buffer and method
6,600,343	07/29/2003	High speed low power input buffer
6,597,600	07/22/2003	Offset compensated sensing for magnetic random access memory
6,577,525	06/10/2003	Sensing method and apparatus for resistive memory device
6,567,297	05/20/2003	Method and apparatus for sensing resistance values of memory cells
6,538,473	03/25/2003	High-speed digital signal buffer and method
6,509,245	01/21/2003	Electronic device with interleaved portions for use in integrated circuits
6,504,750	01/7/2003	Resistive memory element sensing using averaging
6,483,347	11/19/2002	High-speed digital signal buffer and method
6,445,231	09/03/2002	Digital dual-loop DLL design using coarse and fine loops
6,424,684	07/23/2002	Method and apparatus for receiving synchronous data
6,410,955	06/25/2002	Comb-shaped capacitor for use in integrated circuits
6,407,588	06/18/2002	High-speed, low-power input buffer
6,316,976	11/13/2001	Method and apparatus for improving the performance of digital delay locked loop circuits
6,256,234	07/03/2001	Low skew differential receiver with disable feature
6,104,209	08/15/2000	Low skew differential receiver with disable feature
6,069,506	05/30/2000	Method and apparatus for improving the performance of digital delay locked loop circuits
6,026,051	02/15/2000	Low skew differential receiver with disable feature
6,026,050	02/15/2000	Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same (continuation)
5,953,284	09/14/1999	Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same
5,953,276	09/14/1999	Fully-differential amplifier
5,909,201	06/1/1999	Timing Control for a Matrixed Scanned Array
5,894,293	04/13/1999	Field emission display having pulsed capacitance current control
5,874,830	02/23/1999	Adaptively biased voltage regulator and operating method
5,818,365	10/01/1998	Serial to Parallel Conversion with a Phase-Locked Loop
5,638,085	06/10/1997	Timing Control for a Matrixed Scanned Array
5,614,856	03/25/1997	Waveshaping circuit generating two rising slopes for a sense amplifier pulldown device

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<u>Patent Number</u>	<u>Date Issued</u>	<u>Title</u>
5,598,156	01/28/1997	Serial to Parallel Conversion with a PLL

Publications

Textbooks Authored:

- Baker, R.J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 978-0471227540 (first edition, 2002)
- Keeth, B., R.J. Baker, B. Johnson, and F. Lin "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, 201 pages. ISBN: 978-0-470-18475-2
- Baker, R.J., "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1039 pages. ISBN 978-0470229415 (revised second edition, 2008) and ISBN 0-47170055X (second edition, 2005) **Over 30,000 copies of this book's three editions in print.**
- Keeth, B. and R.J. Baker, "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, 201 pages. ISBN 0-7803-6014-1
- Baker, R.J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 978-0780334168

Books, other (edited, chapters, etc.):

- Saxena, V. and Baker, R.J. "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J.D. Irwin and B.D. Wilamowski, *CRC Press*, 2009 second edition.
- Li, H.W., Baker, R.J., and Thelen D., "CMOS Amplifier Design," chapter 19 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)
- Baker, R.J. "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 1999. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)
- Baker, R.J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 1999. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Refereed Journal Papers:

- Estrada, D., Ogas, M.L., Southwick III, R.G., Price, P.M., Baker, R. J., Knowlton, W.B., *Impact of Single pMOSFET Dielectric Degradation on NAND Circuit Performance* (2008), *Microelectronics Reliability*, Vol. 48, No. 3, pp 354-363.
- Leslie, M.B., and Baker, R.J., (2006) "Noise-Shaping Sense Amplifier for MRAM Cross-Point Arrays," *IEEE Journal of Solid State Circuits*, Vol. 41, No. 3, pp. 699-704.
- Hess, H.L., and R.J. Baker., (2000) "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOS Devices," *IEEE Transactions on Power Electronics*, Vol. 15, No. 5, pp. 923-930.

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- Lin, F., Miller J., Schoenfeld A., Ma, M. and Baker, R.J., (1999) "A Register-Controlled Symmetrical DLL for Double-Data-Rate DRAM," *IEEE Journal of Solid State Circuits*, Vol. 34, No. 4, pp. 565-568.
- Bruce, J.D., Li H.W., Dallabetta, M.J. and Baker, R.J., (1996) "Analog layout using ALAS!" *IEEE Journal of Solid State Circuits*, Vol. 31, No. 2, pp. 271-274.
- Li H.W., Dallabetta M.J., and Baker R.J. (1995) "An interactive impulse response extraction system," *Review of Scientific Instruments* 66(10), 5092-5095.
- Ward, S.T., Baker, R.J. and Li. H.W., (1995) "A microchannel plate image intensifier gating circuit capable of pulse widths from 30 ns to 10 us," *Measurement Science and Technology*, Vol. 6, No. 11, pp. 1631-1633.
- Keeth, B., R. J. Baker, and H. W. Li., (1995) "CMOS transconductor VCO with adjustable operating and center frequencies," *Electronics Letters* 31(17), 1397-98.
- Baker, R. J., (1994) "Time domain operation of the TRAPATT diode for picosecond-kilovolt pulse generation," *Review of Scientific Instruments* 65(10), 3286-88.
- Baker, R. J. and S. T. Ward, (1994) "Designing nanosecond high voltage pulse generators using power MOSFETs," *Electronics Letters* 30(20), 1634-35.
- Baker, R. J. and B. P. Johnson, (1994) "Sweep circuit design for a picosecond streak camera," *Measurement Science and Technology* 5(4).
- Baker R. J., D. J. Hodder, B. P. Johnson, P. C. Subedi, and D. C. Williams, (1993) "Generation of kilovolt-subnanosecond pulses using a nonlinear transmission line" *Measurement Science and Technology* 4(8), 893-95.
- Baker R. J. and Johnson B. P., (1993) "Series operation of power MOSFETs for high speed, high voltage switching applications," *Review of Scientific Instruments* 65(6).
- Baker R. J. and Johnson B. P., (1993) "Applying the Marx bank circuit configuration to power MOSFETs," *Electronics Letters* 29(1), 56-57.
- Baker R. J. and Johnson B. P., (1992) "Stacking power MOSFETs for use in high speed instrumentation," *Review of Scientific Instruments* 63(12), 5799-5801.
- Baker R. J. and Johnson B. P., (1992) "A 500 Volt nanosecond pulse generator using cascode connected power MOSFETs," *Measurement Science and Technology* 3 (8), 775-77.
- Baker R. J., Perryman G. T., and Watts P. W., (1991) "A fiber-optically triggered avalanche transistor," *IEEE Transactions on Instrumentation and Measurement* 40(3), 649-52.
- Baker R.J. (1991) "High voltage pulse generation using current mode second breakdown in a bipolar junction transistor," *Review of Scientific Instruments* 62(4), 1031-1036.
- Baker R.J. and Pocha, M.D. (1990) "Nanosecond switching using power MOSFETs," *Review of Scientific Instruments* 61(8), 2211-2213.

Invited Talks and Seminars

Over 30 invited talks at conferences and Universities including: Carnegie Mellon University, Hong Kong University of Science and Technology, Iowa State University, University of Alabama, University of Arkansas, Utah State University, University of Nevada, Las Vegas, University of Idaho, University of Nevada, Reno, Arizona State University, University of Macau, University of Maryland, Temple University, IEEE

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Electron Devices Conference (NVMTS), the Franklin Institute, National Semiconductor, AMI semiconductor, Micron Technology, Rendition, Sun Microsystems, Tower (Israel), Foveon, ICySSS keynote, etc.

Referred Conference Papers and Magazine Articles:

- Regner, J., Balasubramanian, M., Cook, B., Li, Y., Kassayebetre, H., Sharma, A., Baker, R.J., Campbell, K.A., “Integration of IC Industry Feature Sizes with University Back-End-of-Line Post Processing: Example Using a Phase-Change Memory Test Chip,” *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 28-31, April 2009.
- Gupta, S. Saxena, V., Campbell, K.A., and Baker, R.J., “W-2W Current Steering DAC for Programming Phase Change Memory,” *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 59-62, April 2009.
- Rapole, H., Rajagiri, A., M. Balasubramanian, Campbell, K.A., and Baker, R.J., “Resistive Memory Sensing Using Delta-Sigma Modulation,” *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 63-66, April 2009.
- Kassayebetre, H., Regner, J., Rajagiri, A., Sharma, A., Hay, R.R., Baker, R.J., and Campbell, K.A., “Surface Acoustic Wave Device Fabrication using Zinc Oxide and Chalcogenide Thin Films,” poster presentation at the *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April, 2009.
- Ande, H.K., Busa, P., Balasubramanian, M., Campbell, K.A., and Baker, R.J., (2008) A New Approach to the Design, Fabrication, and Testing of Chalcogenide-Based Multi-State Phase-Change Nonvolatile Memory, *proceedings of the 51st Midwest Symposium on Circuits and Systems*, pp. 570-573, August 10-13, 2008.
- Saxena, V., and Baker, R.J., (2008) Compensation of CMOS Op-Amps using Split-Length Transistors, *proceedings of the 51st Midwest Symposium on Circuits and Systems*, pp. 109-112, August 10-13, 2008.
- Saxena, V., and Baker, R.J., (2008) Indirect Compensation Technique for Low-Voltage Op-Amps, *proceedings of the 3rd Annual Austin Conference on Integrated Systems and Circuits (ACISC)*, May 7-9, 2008.
- Cahoon, C., and Baker, R.J., (2008) Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References, *proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 16-19, April 2008.
- Saxena, V., and Baker, R. J., (2006) *Indirect Feedback Compensation of CMOS Op-Amps*, *proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 3-4, April 2006.
- Duvvada, K., Saxena, V., and Baker, R. J., (2006) *High Speed Digital Input Buffer Circuits*, *proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 11-12, April 2006.
- Saxena, V., Plum, T.J., Jessing, J.R., and Baker, R. J., (2006) *Design and Fabrication of a MEMS Capacitive Chemical Sensor System*, *proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 17-18, April 2006.

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- Gorseth, T.L., Estrada, D., Kiepert, J., Ogas, M.L., Cheek, B.J., Price, P.M., Baker, R.J. Bersuker, G., Knowlton, W.B., *Preliminary Study of NOR Digital Response to Single pMOSFET Dielectric Degradation*, presented at the Workshop on Microelectronic Devices (Boise, Idaho; April 14, 2006)
- Gribb, M., Plumlee, D., Moll, A., Hill, H., Hong, F., Baker, J., Loo, S.M., Walters, R. and Imonigie, J., (2006) *An In-Situ Ion Mobility Spectrometer Sensor System for Detecting Gaseous VOCs in the Vadose Zone, Fourth International Conference on Unsaturated Soils (UNSAT '06) Conference, April 2-6, 2006, Carefree, AZ.*
- Gribb, M., H. Hill, J. Baker, S.M. Loo, A. Moll, (2005), *Ion Mobility Spectrometer (IMS) Sensor Project*, presented at the Environmental & Subsurface Science Symposium, Inland Research Alliance, Sept. 19-21, 2005, Big Sky, Montana.
- Ogas, M.L., Price, P.M., Kiepert J., Baker R.J., Bersuker G., and Knowlton W.B., (2005) *Degradation of Rise Time in NAND Gates Using 2.0 nm Gate Dielectrics*, oral presentation and publication at the 2005 IEEE Integrated Reliability Workshop, October 2005.
- Butler, D.L, and R.J. Baker, (2005) *Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes*, 2005 Midwest Symposium on Circuits and Systems.
- Cheek, B.J., R.G. Southwick III, M.L. Ogas, P.E. Nagler, D. Whelchel, S. Kumar, R. J. Baker, W.B. Knowlton, (2004) *Preliminary Soft Breakdown (SBD) Effects In CMOS Building Block Circuits*, poster presentation at 2004 IEEE International Integrated Reliability Workshop, Oct. 18-21.
- Ogas, M., R. Southwick, B. Cheek, C. Lawrence, S. Kumar, A. Haggag, R. J. Baker, and W. B. Knowlton, (2004) *Multiple Waveform Pulse Voltage Stress Technique for Modeling Noise in Ultra Thin Oxides*, poster presentation at Workshop on Microelectronics and Electron Devices, Boise, Idaho, April 16, 2004.
- Ogas, M. L., R. G. Southwick III, B. J. Cheek, R. J. Baker, G. Bersuker, W. B. Knowlton, (2004) *Survey of Oxide Degradation in Inverter Circuits Using 2.0nm MOS Devices*, in proceedings of the 2004 IEEE International Integrated Reliability Workshop, pp. 32-36.
- Cheek, Betsy J., Nate Stutzke, Kumor Santosh , R. Jacob Baker, Amy J. Moll and William B. Knowlton, (2004) *Investigation of Circuit-Level Oxide Degradation and its Effect on CMOS Inverter Operation Performance and MOSFET Characteristics*, 2004 IEEE International Reliability Physics Symposium, April, 25-29.
- Stutzke, Nate, Betsy J. Cheek, Miles Wiscombe, Terry Lowman, Santosh Kumar, R. Jacob Baker, Amy J. Moll and William B. Knowlton, (2003) *Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics*, 2003 IEEE International Integrated Reliability Workshop, Oct, 20-23.
- Ogas, M. L., R. G. Southwick, B. J. Cheek, C. E. Lawrence, S. Kumar, A. Haggag, R. J. Baker, W. B. Knowlton (2003) *Investigation of Multiple Waveform Pulse Voltage Stress (MWPVS) Technique in Ultra-Thin Oxides*, poster presentation at the 2003 IEEE International Integrated Reliability Workshop Oct, 20-23.
- Baker, R.J., (2003) *Mixed-Signal Design in the Microelectronics Curriculum*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2.
- J.A. Hartman, R.J. Baker, M. Gribb, H.H. Hill, J. Jessing, A. Moll, W. Prouty, D. Russell, (2003) *A Miniaturized Ion Mobility Spectrometer (IMS) Sensor for Wireless Operation*,

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- FAME (Frontiers in Assessment Methods for the Environment) Symposium, Sponsored by NSF, Minneapolis, Minnesota, August 10-13, 2003.
- Lawrence, C.E., B.J. Cheek, T.E. Lawrence, Santosh Kumar, A. Haggag, R.J. Baker, and W.B. Knowlton, (2003) *Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2.
 - Betsy Cheek, Carrie Lawrence, Tim Lawrence, Jose Gomez, Theodora Caldwell, Dorian Kiri, Santosh Kumar, Jake Baker, Amy J. Moll, and William B. Knowlton, (2002) *Gate Dielectric Degradation Effects on nMOS Devices and Simple IC Building Blocks (SICBBs)*, IEEE Electron Devices Society Boise Meeting, Boise, ID Oct. 25.
 - Lawrence, C., B. Cheek, T. Caldwell, T. Lawrence, D. Kiri, S. Kumar, J. Baker, A. J. Moll and W. B. Knowlton, (2002) *Pulse voltage stressing of ultrathin gate oxides in NMOS devices, poster session at IEEE International Integrated Reliability Workshop*, October 21-24.
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- Baker, R.J., (1990) "Step-recovery diodes sharpen pulses," *Engineering Design News Magazine*, pp. 154-156, May 10.

Education

<u>Year</u>	<u>College/University</u>	<u>Degree</u>
1993	University of Nevada, Reno	Ph.D., Electrical Engineering
1988	University of Nevada, Las Vegas	MS, Electrical Engineering
1986	University of Nevada, Las Vegas	BS, Electrical Engineering

Membership in Professional and Scholarly Organizations:

- Member, ASEE
- Member, IEEE (student, 1983; member, 1988; senior member, 1997), Societies: Circuits and Systems, Education, Instrumentation and Measurement, Solid State Circuits
- Licensed Professional Engineer

Honors and Awards

- Frederick Emmons Terman Award from the American Society of Engineering Education – 2007.
- President's Research and Scholarship Award, Boise State University – 2005.
- Honored Faculty Member – Boise State University Top Ten Scholar/Alumni Association 2003.
- Outstanding department of electrical engineering faculty, Boise State 2001.
- 2000 prize paper award from the IEEE Power Electronics Society.
- University of Idaho, Department of electrical engineering outstanding researcher award, 1998-99.
- University of Idaho, College of engineering outstanding young faculty award, 1996-97.

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