

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

**Krishna Shenai, Ph.D.**

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**Expertise**

- MOS and Bipolar Device Technology
  - VLSI Metallization and Interconnect Technology
  - Semiconductor Technology
  - Computer-Aided Design (STCAD)
  - Device and Process Simulation
  - Semiconductor Device and Circuit Modeling
  - Microchip Fabrication & Analysis
  - Power Semiconductor Devices
  - Power Management
  - RF and Microwave Devices
  - Sensors and Medical Devices
  - Electronics Packaging and Assembly
  - Reliability of Power Systems
  - Semiconductor Device Physics
  - CMOS, DMOS and BiCMOS
  - Silicon Carbide & GaN Technology
  - Power Converters & Inverters
  - Smart Power Grid
  - Renewable Energy Technology
  - Power Transmission & Distribution
  - Environmental Sensing
  - Ecosystem Monitoring & Modeling
  - Low Power Mixed Signal Electronics
  - RFIC, MMIC and OEIC
  - Wireless Sensor Networks
  - Semiconductor Processing
  - Electrical and Electronic Failures
  - Robotic Surgery
  - Biomedical Instrumentation
  - Patents and Trademarks
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**Professional Summary**

Dr. Shenai has over 30 years of combined industry, research, academic, consulting and entrepreneurial experience. His research covers the physics and technology of semiconductor devices and integrated circuits used for signal and power processing, sensors and wireless sensor networks, semiconductor manufacturing, power electronics, robotic surgery, RF and microwave electronics, power management, power transmission and distribution systems, smart power grid, environmental monitoring and control, and electronics system failures and reliability. He is a named inventor in 12 issued US patents and over 40 international patents, and has authored or co-authored over 350 peer-reviewed publications of which more than 100 are in IEEE journals. He has also edited 3 books and contributed to 8 book chapters. He is a Fellow of IEEE, a Fellow of AAAS, a Fellow of IETE (India), a Distinguished Lecturer of IEEE Electron Devices Society, and a member of the Yugoslavian National Academy of Engineering.

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**Consultant Curriculum Vitae**

**Employment History**

From: 2007      **University of Toledo**  
To: Present      Toledo, OH  
Position: *2007-Present: Professor, Electrical Engineering and Computer Science Department*  
*2007-2009: Chairman, Electrical Engineering and Computer Science Department*  
Performing teaching and research on the physics, technology, and application of power semiconductor devices and power converters, low-power RF micro-systems, wireless sensors and sensor networks, intelligent systems, robotic surgery, and device and circuit modeling.

From: 1996      **LoPel Corporation**  
To: Present      Naperville, IL  
Position: *Co-Founder & Vice President*  
Consulting firm specializing in technology and intellectual property consulting.

From: 2006      **Utah State University**  
To: 2007      Logan, UT  
Position: *First Utah Science, Technology and Research (USTAR) Endowed Professor on Intelligent Systems, Electrical and Computer Engineering Department*  
Performed teaching and research on the physics, technology, and application of power semiconductor devices and power converters, low-power RF micro-systems, wireless sensors and sensor networks, intelligent systems, and device and circuit modeling.

From: 2004      **Zeus Semiconductor, Inc.**  
To: 2005      Lisle, IL  
Position: *Co-Founder, Director & CTO*

From: 2002      **Shakti Systems, Inc.**  
To: 2003      Lisle, IL  
Position: *Founder, Chairman & CEO/CTO*

From: 1995      **University of Illinois at Chicago**  
To: 2004      Chicago, IL  
Position: *1998-2004: Professor, Electrical and Computer Engineering*

## **Silicon Valley Expert Witness Group, Inc. Consultant Curriculum Vitae**

*1995-1998: Associate Professor, Electrical Engineering and  
Computer Science Department*

Performed teaching and research on the physics, technology, and application of power semiconductor devices and power converters, low-power RF micro-systems, wireless technology, and device and circuit modeling.

From: 1993      **University of Wisconsin**  
To: 1995      Madison, WI  
Position: *Assistant Professor, Electrical and Computer Engineering  
Department*

Performed teaching and research on the physics, technology, and application of GaAs MMIC, sub-micron VLSI devices and integrated circuits, and power semiconductor devices and high-voltage integrated circuits.

From: 1990      **Intel Corporation**  
To: 1993      Hillsboro, OR  
Position: *Senior Staff Engineer*

Developed 0.5/0.35 micron CMOS/BiCMOS technology for advanced low-power mixed-signal high-speed microprocessor applications. Specific tasks included:

- Design, characterization, and modeling of 0.5/0.35 micron bipolar and CMOS devices
- Development of advanced bipolar and CMOS circuit simulation models
- Design of high-speed logic standard cells
- Interfacing/consulting with process development, Q&R and logic design groups

From: 1986      **General Electric Corporation**  
To: 1990      Schenectady, NY  
Position: *Device Physicist, Corporate R&D Center*

Pioneered the development of low-voltage power MOS technologies for discrete and smart-power applications using advanced device structures, refractory metallization, multilevel interconnects, and silicon trenches. Specific tasks included:

- Conception, modeling, design, testing, and system implementation of low-voltage power MOS devices for both discrete and smart-power applications
- Development of circuit simulation models for semiconductor devices, and magnetic and passive devices
- Interfacing with circuit design groups to implement advanced power electronic systems such as high-frequency high-

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density power supplies, multi-lux lamp ballasts, display drivers, high-speed ultrasound systems, automotive electronics, aircraft electronics, radar communication systems, computer controllers, and, so forth

- Developed the process technology for advanced power MOSFETs, power rectifiers, and 300V smart-power IC's using high-speed power BiCMOS devices.
- Integrated advanced MOS gates in high-power devices such as IGBT's and MCT's
- Investigated the feasibility of high-temperature (up to 300°C) operation of 600V IGBT and MCT modules including high-speed BiCMOS gate drivers
- Conceived and modeled GaAs, SiC, and diamond power devices for future high-speed, high-power, and high-temperature applications
- Participated in sponsored contract projects with Wright Patterson AFB, Naval Ocean Systems Center (NOSC), NASA, DARPA, Apple Computers, IBM, and other GE internal business units
- Supervised several technicians, junior device/process engineers, and university summer and coop students

From: 1983      **Stanford University**  
To: 1986      Stanford, CA  
Position: *Research Assistant, Integrated Circuits Laboratory, EE Department*  
Worked on Ph.D. thesis research on surface and interface related physics of GaAs MESFET's and Schottky barriers fabricated using ion-implantation and insitu MBE. Developed physical device models for GaAs MESFET's, Schottky diodes, and ohmic contacts using advanced physical concepts and extensive experimental results. Developed models for Si Schottky barriers to refractory moralizations using CVD tungsten and silicides based on Ti, Pt, and tungsten.

From: 1981      **COMSAT Laboratories**  
To: 1983      Clarksburg, MD  
Position: *Member, Technical Staff*  
Developed ultra low noise high-gain cryogenically cooled GaAs MESFET amplifiers for application in broadband satellite communication systems. Specific tasks included: modeling, design, and characterization of GaAs devices and micro strip circuits built on fused silica, alumina, and GaAs substrates for MMIC applications. Developed circuit simulation models for several passive and active components (including FET's, couplers, CPW

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Consultant Curriculum Vitae**

transitions, inter digitated capacitors, and spiral inductors) for use in advanced microwave design software (SCOMPACT). Supervised technicians, junior engineers, and coop graduate students.

From: 1979      **University of Maryland**  
To: 1981      College Park, MD  
Position: *Graduate Assistant, Electrical and Computer Engineering Department*

**Patents**

<u>Patent Number</u>	<u>Date Issued</u>	<u>Title</u>
6,844,251	01/18/2005	Method of forming a semiconductor device with a junction termination layer
6,819,088	11/16/2004	DC-DC converter with resonant gate drive
6,791,341	09/14/2004	Current derivative sensor
6,791,298	09/14/2004	Monolithic battery charging device
6,714,049	03/30/2004	Logic state transition sensor circuit
6,608,503	08/19/2003	Hybrid comparator and method
5,959,439	09/28/1999	Monolithic DC To DC Converter
5,914,513	06/22/1999	Electronically Tunable Capacitor
5,234,851	08/10/1993	Small Cell, Low Contact Assistance Rugged Power Field Effect Devices And Method Of Fabrication
5,119,153	06/02/1992	Small Cell Low Contact Resistance Rugged Power Field Effect Devices And Method Of Fabrication
4,998,151	03/05/1991	Power Field Effect Devices Having Small Cell Size And Low Contact Resistance
4,985,740	01/15/1991	Power Field Effect Devices Having Low Gate Sheet Resistance And Low Ohmic Contact Resistance

**Litigation Support**

2005-2006	<b>Quinn Emanuel Urquhart Oliver &amp;Hedges</b> Case: Siliconix, Inc. v. Denso Corporation Project: Patent Evaluation Status: Closed
2004-2005	<b>Marger, Johnson &amp; McCollom P.C.,</b> Case: IXYS Corporation v. Advanced Power Technology Project: Patent litigation, testifying witness Status: Closed
2000-2001	<b>Townsend and Townsend and Crew</b> Case: International Rectifier v. IXYS Corporation Project: Patent litigation, testifying witness

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Consultant Curriculum Vitae**

Status: Closed

1998-1999

**Coudert Brothers**

Case International Rectifier v. Samsung Semiconductor & Samsung Electronics Co.

Project: Patent litigation, testifying witness

Status: Closed

1997-1998

**McBreen, McBreen & Kopko**

Case Beilfuss v. Thermatool

Project: Testifying witness

Status: Closed

1997-1998

**Coudert Brothers and Bird & Bird**

Case International Rectifier v. SGS Thomson Microelectronics

Project: Patent litigation, testifying witness

Status: Closed

1995-1998

**O'Melveny and Myer & Coudert Brothers**

Case International Rectifier v. SGS Thomson Microelectronics

Project: Patent litigation, testifying witness

Status: Closed

**Education**

<u>Year</u>	<u>College/University</u>	<u>Degree</u>
1986	Stanford University, Stanford, CA	Ph.D., Electrical Engineering
1981	University of Maryland, College Park, MD	MSEE
1979	Indian Institute of Technology, Madras, India	B. Tech. in Electronics

**Publications**

**Books**

- 1) K. Shenai, Editor, *VLSI Metallization Technologies*, Artech House, Norwood, MA, 1990.
- 2) A. Selvarajan, K. Shenai, and V. K. Tripathi, Eds., *Optoelectronics: Technologies and Applications*, ISBN 0-8194-1213-9 and ISBN 0-8194-1209-0 (pbk.), SPIE Press, Bellingham, WA, 1993.
- 3) A. Selvarajan and K. Shenai, Eds., *Optoelectronics: Current Trends*, Tata McGraw Hill, 1996, ISBN 0-07-462455-5.

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## Consultant Curriculum Vitae

### Conference Proceedings

- 1) Co-Editor, *High-Frequency Power Conversion Conference*, Intertec Communications, Ventura, CA, 1989.
- 2) C. McConica, R. Blewer and K. Shenai, *MRS Proc. Tungsten and Other Refractory Metals for ULSI V*, Materials Research Society, Pittsburgh, PA, 1989.
- 3) A. Selvarajan, B. S. Sonde, K. Shenai, and V. K. Tripathi, Eds., *Proc. Conf. Emerging Optoelectronic Technologies (CEOT)*, Tata-McGraw Hill, ISBN 0-07-462397-4, New Delhi, India, 1992.
- 4) T. Kwok, T. Kikkawa and K. Shenai, Eds., *SPIE Proc. Submicron Metallization*, SPIE, Bellingham, WA, 1993.
- 5) A. Selvarajan, B. S. Sonde, K. Shenai, and V. K. Tripathi, Eds., *Proc. Conf. Emerging Optoelectronic Technologies (CEOT)*, Tata-McGraw Hill, ISBN 0-07-462397-4, New Delhi, India, 1994.

### Book Chapters

- [1] M. Trivedi, S. Pendharkar and K. Shenai, "Overview: Devices and Components," in *The Industrial Electronics Handbook*, J. D. Irwin, Editor-in-Chief, IEEE/CRC Press, 1997, ISBN0-8493-8343-9.
- [2] E. McShane and K. Shenai, "VLSI Technology: A Systems Perspective," in *The VLSI Handbook*, W.-K. Chen, Editor-in-Chief, IEEE/CRC Press, 2000, ISBN 0-8493-8593-8.
- [3] P. Khandelwal and K. Shenai, "Microelectronics Packaging," in *The VLSI Handbook*, W.-K. Chen, Editor-in-Chief, IEEE/CRC Press, 2000, ISBN 0-8493-8593-8.
- [4] K. Shenai, K. F. Galloway, and R. D. Schrimpf, "The Effects of Space Radiation Exposure on Power MOSFETs: A Review," in *Radiation Effects and Soft Errors in Integrated Circuits and Electronic Devices*, R. D. Schrimpf and D. M. Fleetwood, Eds., World Scientific, Singapore, 2004 (**invited**).
- [5] K. Shenai and S. Abedinpour, "Insulated Gate Bipolar Junction Transistors (IGBTs)," in *Power Electronics Handbook*, M. H. Rashid, Editor-in-Chief, Academic Press 2001, ISBN: 0-12-581650-2, pp. 101-116.
- [6] M. Trivedi and K. Shenai, "Power Semiconductor Devices," in *The Electrical Engineering Handbook*, W.-K. Chen, Editor-in-Chief, Elsevier Academic Press 2005, ISBN: 0-12-170960-4, pp. 163-176.
- [7] E. McShane and K. Shenai, "Noise in Analog and Digital Systems," in *The Electrical Engineering Handbook*, W.-K. Chen, Editor-in-Chief, Elsevier Academic Press 2005, ISBN: 0-12-170960-4, pp. 101-108.
- [8] K. Shenai, M. Peralta, S. Mukhopadhyay, and R. Bharadwaj, "Smart Sensor Networks," Chapter 12, in *Selected Topics in Communication Networks and Distributed Systems*, S. Misra, Editor, World Scientific Publishing Company, Singapore, February 2, 2009.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

**Archived Journal Papers**

- [1] K. Shenai and H. C. Lin, "CAD Modeling of Diffused p-n Junctions," *COMPEL, The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, vol. 1, no. 2, pp. 111-127, June 1982.
- [2] K. Shenai, "Depletion Layer Calculations and Modeling of a Single-Diffused p-n Junction with Complementary Error Function Profile," *COMPEL, The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, vol. 1, no. 3, pp. 175-186, June 1982.
- [3] K. Shenai and H. C. Lin, "Analytical Solutions for Avalanche Breakdown Voltages of Single-Diffused Gaussian Junctions," *Solid-State Electron.*, vol. 26, no. 3, pp. 211-216, March 1983.
- [4] K. Shenai, "Analytical Solutions for Threshold Voltage Calculations in Ion-Implanted MOSFETs," *Solid-State Electron.*, vol. 26, no. 8, pp. 761-766, August 1983.
- [5] K. Shenai and H. C. Lin, "Transient Response of Diffused Junction Capacitors," *IEEE Trans. Electron Devices*, vol.30, no. 10, pp. 1409-1411, October 1983.
- [6] K. Shenai, "Orientation Dependence of Avalanche Breakdown Voltage in GaAs with Non-Uniform Doping Profiles," *Solid-State Electron.*, vol. 27, no. 1, pp. 107-108, January 1984.
- [7] K. Shenai, E. Sangiorgi, K. C. Saraswat, R. M. Swanson, and R. W. Dutton, "Accurate Barrier Modeling of Metal and Silicide Contacts," *IEEE Electron Device Lett.*, vol. 5, no. 5, pp.145-147, May 1984.
- [8] K. Shenai, S. J. Eglash, R. W. Dutton, M. Zurakowski, and W. E. Spicer, "Field-Enhanced Tunneling and Barrier Lowering in Al-nGaAs-nGaAs Schottky Contacts Grown by MBE," *IEEE Electron Device Lett.*, vol. 5, no. 8, pp. 329-332, August 1984.
- [9] K. Shenai, E. Sangiorgi, R. M. Swanson, K. C. Saraswat, and R. W. Dutton, "Modeling and Characterization of Dopant Redistributions in Metal and Silicide Contacts," *IEEE Trans. Electron Devices*, vol. 32, no. 4, pp. 793-799, April 1985.
- [10] K. Shenai and R. W. Dutton, "A New Interpretation of the Channel Charge Control Mechanism in GaAs MOSFETs," *IEEE Electron Device Lett.*, vol. 6, no. 10, pp. 528-530, October 1985.
- [11] K. Shenai and R. W. Dutton, "Low-Field Channel Pinch-Off Mechanism in GaAs MOSFETs," *IEEE Trans. Electron Devices*, vol. 32, no. 11, pp. 2550-2551, November 1985.
- [12] K. Shenai, R. W. Dutton, and S. J. Eglash, "Improved Physics of Ohmic Contacts to Semiconductors," *IEEE Trans. Electron Devices*, vol. 33, no. 11, pp. 1866-1867, November 1986.
- [13] S. J. Eglash, N. Newman, S. Pan, D. Mo, K. Shenai, W. E. Spicer, F. A. Ponce, and D. M. Collins, "Engineered Schottky Barrier Diodes for the Modification and Control of Schottky Barrier Heights," *J. Appl. Phys.*, vol. 61, pp. 5159-5169, June 1987.
- [14] K. Shenai, "Very Low Resistance Non-Alloyed Ohmic Contacts to Sn-Doped Molecular Beam Epitaxial GaAs," *IEEE Trans. Electron Devices*, vol. 34, no. 8, pp. 1642-1649, August 1987.
- [15] K. Shenai and R. W. Dutton, "Current Transport Mechanisms in Atomically Abrupt Metal-Semiconductor Interfaces," *IEEE Trans. Electron Devices*, vol. 35, no. 4, pp. 468-482, April 1988.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [16] K. Shenai, and R. W. Dutton, "Low-Field Electron Transport Mechanisms in GaAs MOSFETs," *IEEE Trans. Electron Devices*, vol. 35, no. 5, pp. 578-589, May 1988.
- [17] K. Shenai and R.W. Dutton, "Channel-Buffer (Substrate) Interface Phenomena in GaAs MOSFETs Fabricated by MBE," *IEEE Trans. Electron Devices*, vol. 35, no. 5, pp. 590-603, May 1988.
- [18] K. Shenai, P. A. Piacente, R. Saia, C. S. Korman, W. Tantraporn, and B. J. Baliga, "Ultralow Resistance, Selectively Silicided VDMOS FETs for High-Frequency Power Switching Applications Fabricated Using Sidewall Oxide Spacer Technology," *IEEE Trans. Electron Devices*, vol. 35, no.12, pp. 2459, December 1988.
- [19] K. Shenai, P. A. Piacente, N. Lewis, G. A. Smith, M. D. McConnell, and B. J. Baliga, "Formation and Properties of Rapid Thermally Annealed TiSi<sub>2</sub> on Lightly Doped and Heavily Implanted Silicon," *J. Vac. Sci. Technol. B* 6(6), pp. 1728-1733, November-December 1988.
- [20] K. Shenai, P. A. Piacente, C. S. Korman, and B. J. Baliga, "Selectively Silicided Vertical Power DMOS FET's for High-Frequency Power Switching Applications," *J. Vac. Sci. Technol. B* 6(6), pp.1740-1745, November-December 1988.
- [21] K. Shenai, C. S. Korman, B. J. Baliga, and P. A. Piacente, "A 50-V, 0.7-mΩ·cm<sup>2</sup> Vertical Power DMOSFET," *IEEE Electron Device Lett.*, vol. 10, no. 3, pp. 101-103, March 1989.
- [22] K. Shenai, P. A. Piacente, C. S. Korman, and B. J. Baliga, "High Performance Vertical Power DMOSFETs with Selectively Silicided Gate and Source Regions," *IEEE Electron Device Lett.*, vol.10, no. 4, pp. 153-155, April 1989.
- [23] K. Shenai, P. A. Piacente, R. Saia, and B. J. Baliga, "Blanket LPCVD Tungsten Silicide Technology for Smart-Power™ Applications," *IEEE Electron Device Lett.*, vol. 10, no. 6, pp. 270-273, June 1989.
- [24] K. Shenai, P. A. Piacente, R. Saia, C. S. Korman, and B. J. Baliga, "Selectively Silicided Vertical Power DMOSFETs for High-Frequency Power Conversion," *Electronics Lett.*, vol. 25, no.12, pp.784-785, June 1989.
- [25] K. Shenai, "High-Frequency Power MOSFETs Fabricated Using Selectively Deposited LPCVD Tungsten," *Electronics Lett.*, vol.25, no. 16, pp. 1033-1034, August 1989.
- [26] K. Shenai, R. S. Scott, and B. J. Baliga, "Optimum Semiconductors for High-Power Electronics," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1811-1823, September 1989.
- [27] K. Shenai, "Optimally Scaled Low-Voltage Vertical Power DMOSFETs for High-Frequency Power Switching Applications," *IEEE Trans. Electron Devices*, vol. 37, no. 4, pp. 1141-1153, April 1990.
- [28] K. Shenai and B. J. Baliga, "Monolithically Integrated Power MOSFET and Schottky Diode with Reduced Reverse Recovery Transient," *IEEE Trans. Electron Devices*, vol. 37, no. 4, pp.1167-1169, April 1990.
- [29] K. Shenai, "Effect of Gate Resistance on the High-Frequency Switching Efficiencies of Advanced Power MOSFETs," *IEEE J. Solid-State Circuits*, vol. 25, no. 5, pp. 595-601, April 1990.
- [30] K. Shenai, "Novel Refractory Contact and Interconnect Metallizations for High-Voltage and Smart-Power™ Applications," *IEEE Trans. Electron Devices*, vol. 37, no. 10, pp.2207-2221, October 1990.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [31] K. Shenai, "Potential Impact of Emerging Semiconductor Technologies on Advanced Power Electronic Systems," *IEEE Electron Device Lett.*, vol. 11, no. 11, pp. 520-522, November 1990.
- [32] K. Shenai, "Gate-Resistance Limited Switching Frequencies of Power MOSFETs," *IEEE Electron Device Lett.*, vol. 11, no. 11, pp. 544-546, November 1990.
- [33] K. Shenai, "Manufacturability Issues Related to Transient Thermal Annealing of Titanium Films in a Rapid Thermal Processor," *IEEE Trans. Semiconductor Manufacturing*, vol. 4, no. 1, pp. 1-8, February 1991.
- [34] K. Shenai, "A Study of Structural, Electrical, and Optical Properties of Low-Pressure Chemical Vapor Deposited Tungsten Silicide Films Processed at Elevated Temperatures," *J. Appl. Phys.*, vol. 69, pp.3646-3652, March 1991.
- [35] K. Shenai, "A 55-V, 0.2-m $\Omega$ -cm<sup>2</sup> Vertical Trench Power MOSFET," *IEEE Electron Device Lett.*, vol. 12, no. 3, pp. 108-110, March 1991.
- [36] G. A. Smith, K. Shenai, N. Lewis, and P. A. Piacente, "The Role of SIMS and RBS in Advanced Metallization Development," *J. Inst. Electronics and Telecommunications Engineers (India)*, vol.37, no. 2, pp. 235-241, March-April 1991.
- [37] N. Lewis, K. Shenai, G. A. Smith, and P. A. Piacente, "High Resolution TEM in Metallization," *J. Inst. Electronics and Telecommunications Engineers (India)*, vol. 37, no. 2, pp. 223-234, March-April 1991.
- [38] K. Shenai, "An Overview of Metallization Technologies for High-Voltage and Smart-Power™ Applications," *J. Inst. Electronics and Telecommunications Engineers (India)*, vol. 37, no. 2, pp.187-193, March-April 1991.
- [39] K. Shenai, "Characteristics of LPCVD WSi<sub>2</sub>/n-Si Schottky Contacts," *IEEE Electron Device Lett.*, vol. 12, no. 4, pp. 169-171, April 1991.
- [40] K. Shenai, "Performance Potential of Low-Voltage Power MOSFETs in Liquid-Nitrogen Cooled Power Systems," *IEEE Trans. Electron Devices*, vol. 38, no. 4, pp. 934-936, April 1991.
- [41] K. Shenai, "Interelectrode Capacitance Nonlinearities of Vertical Power DMOSFETs," *Electronics Lett.*, vol. 27, no. 3, pp. 280-282, June 1991.
- [42] K. Shenai, "Effect of *p*-base Sheet and Contact Resistances on Static Current-Voltage Characteristics of Vertical Power DMOSFETs," *IEEE Electron Device Lett.*, vol. 12, no. 6, pp. 270-272, June 1991.
- [43] K. Shenai, "Thermal Stability of Titanium Silicide Films on Single Crystal and Polycrystalline Silicon," *J. Mater Res.*, vol. 6, no. 7, pp. 1502-1511, July 1991.
- [44] K. Shenai, "A Circuit Simulation Model for High-Frequency Power MOSFETs," *IEEE Trans. Power Electronics*, vol.6, no. 3, pp. 539-547, July 1991.
- [45] K. Shenai, "Electron Mobility in MOS Channels Formed Along Anisotropically Dry Etched <110> Silicon Trench Side Walls," *Electronics Lett.*, vol. 27, no. 9, pp. 715-717, July 1991.
- [46] K. Shenai, "Nearly Bird's Beak-Free Local Oxidation Technology for Controlled Dielectric Formation in Deep Silicon Trenches," *Electronics Lett.*, vol. 27, no. 8, pp. 637-639, July 1991.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [47] K. Shenai, "Effect of Arsenic Implantation on Electrical Characteristics of LPCVD  $WSi_2/n$ -Si Schottky Contacts," *IEEE Trans. Electron Devices*, vol. 38, no. 9, pp. 2033-2035, September 1991.
- [48] K. Shenai, "Structural and Electrical Properties of Furnace and Rapid Thermally Annealed LPCVD  $WSi_2$  Films on Single-Crystal, Polycrystalline, and Amorphous Silicon Substrates," *IEEE Trans. Electron Devices*, vol. 39, no. 1, pp. 193-199, January 1992.
- [49] K. Shenai, "Silicon Trench Undercutting Caused by the Preferential Plasma Etching of Surface Implanted Regions," *IEEE Trans. Electron Devices*, vol. 39, no. 3, pp. 737-738, March 1992.
- [50] K. Shenai, "Diffusion Profiles of Boron Implanted into Plasma Etched Silicon Surfaces," *IEEE Trans. Electron Devices*, vol. 39, no. 5, pp. 1242-1245, May 1992.
- [51] K. Shenai, "A High-Density, Self-Aligned Power MOSFET Structure Fabricated using Sacrificial Spacer Technology," *IEEE Trans. Electron Devices*, vol. 39, no. 5, pp. 1252-1255, May 1992.
- [52] K. Shenai, "Optimum DMOS Cell Doping Profiles for High-Voltage Discrete and Integrated Device Technologies," *IEEE Trans. Electron Devices*, vol. 39, no. 5, pp. 1255-1257, May 1992.
- [53] K. Shenai, "Optimized Trench MOSFET Technologies for Power Devices," *IEEE Trans. Electron Devices*, vol. 39, no. 6, pp. 1435-1443, June 1992.
- [54] K. Shenai, "A Novel Trench Planarization Technique Using Polysilicon Refill, Polysilicon Oxidation, and Oxide Etchback," *IEEE Trans. Electron Devices*, vol. 40, no. 2, pp. 459-463, February 1993.
- [55] L. Zhang, J. L. Shohet, D. Dallmann, J. H. Booske, P. R. Speth, K. Shenai, M. J. Goeckner, J. B. Kruger, P. Rissman, J. E. Turner, E. Perez-Albuerna, S. Lee, and N. Meyyappan, "Low Energy Separation by Implantation of Oxygen Structures via Plasma Source Ion Implantation," *Appl. Phys. Lett.*, pp. 962-964, August 1994.
- [56] K. Shenai and J. B. Cole, "Special Issue Foreword," *IEEE J. Solid-State Circuits*, Special Issue on High-Speed IC Design, vol. 29, no. 10, pp. 1163-1165, October 1994.
- [57] H. Iwai, C. R. Selvakumar, and K. Shenai, "Special Issue Foreword," *IEEE Trans. Electron Devices* Special Issue on Bipolar BiCMOS/CMOS Devices and Technologies, vol. 42, no. 3, pp. 373-376, March 1995.
- [58] I. Widjaja, A. Kurnia, K. Shenai, and D. M. Divan, "Switching Dynamics of IGBTs in Soft-Switching Inverters," *IEEE Trans. Electron Devices*, vol. 42, no. 3, pp. 445-454, March 1995.
- [59] D. A. Dallmann and K. Shenai, "Scaling Constraints Imposed by Self-Heating in Submicron SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 42, no. 3, pp. 489-496, March 1995.
- [60] K. J. Fischer and K. Shenai, "Effect of Bipolar Turn-on on the Static Current-Voltage Characteristics of Scaled Vertical Power DMOSFETs," *IEEE Trans. Electron Devices*, vol. 42, no. 3, pp. 555-563, March 1995.
- [61] S. Pendharkar, C. Winterhalter, and K. Shenai, "A Behavioral Circuit Simulation Model for High-Power GaAs Schottky Diodes," *IEEE Trans. Electron Devices*, vol. 42, no. 10, pp. 1847-1854, October 1995.
- [62] K. Shenai, "Special Issue Foreword," *IEEE J. Solid-State Circuits*, Special Issue on High-Speed IC Design, vol. 31, no. 1, pp. 2-3, January 1996.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [63] H. H. Li, N. Kutkut, D. Divan, and K. Shenai, "Design Considerations of IGBTs in Resonant Converter Applications," *IEEE J. Solid-State Circuits*, vol. 31, no. 1, pp. 97-105, January 1996.
- [64] S. Pendharkar, M. Trivedi, and K. Shenai, "Dynamics of Reverse Recovery of High-Power P-i-N Diodes," *IEEE Trans. Electron Devices*, vol. 43, no. 1, pp. 142-149, January 1996.
- [65] S. Pendharkar and K. Shenai, "Evaluation of Turn-On Performance of P-i-N Rectifiers and IGBTs under Zero-Voltage Switching," *IEEE Trans. Electron Devices*, vol. 43, no. 4, pp. 647-654, April 1996.
- [66] S. Pendharkar, C. Winterhalter, and K. Shenai, "Modeling and Characterization of the Reverse Recovery of a High-Power GaAs Schottky Diode," *IEEE Trans. Electron Devices*, vol. 43, no. 5, pp. 685-690, May 1996.
- [67] K. Fischer and K. Shenai, "Dynamics of Power MOSFET Switching under Unclamped Inductive Loading Conditions," *IEEE Trans. Electron Devices*, vol. 43, no. 6, pp. 1007-1015, June 1996.
- [68] M. Trivedi, S. Pendharkar, and K. Shenai, "Switching Characteristics of MCTs and IGBTs in Power Converters," *IEEE Trans. Electron Devices*, vol. 43, no. 11, pp. 1994-2003, November 1996.
- [69] K. Fischer and K. Shenai, "Electrothermal Effects During Unclamped Inductive Switching of Power MOSFETs," *IEEE Trans. Electron Devices*, vol. 44, no. 5, pp. 874-878, May 1997.
- [70] S. Pendharkar and K. Shenai, "Optimization of the Anti-Parallel Diode in an IGBT Power Module," *IEEE Trans. Electron Devices*, vol. 44, no. 5, pp. 879-886, May 1997.
- [71] M. Trivedi and K. Shenai, "Modeling the Turn-Off of IGBTs in Hard- and Soft-Switching Power Converters," *IEEE Trans. Electron Devices*, vol. 44, no. 5, pp. 887-893, May 1997.
- [72] M. Trivedi and K. Shenai, "Investigation of the Short-Circuit Performance of an IGBT," *IEEE Trans. Electron Devices*, vol. 45, no. 1, pp. 313-320, January 1998.
- [73] M. Trivedi, A. Mulay, R. Vijayalakshmi, and K. Shenai, "Mixed Mode Simulation of Power Converters," *TCAD Driven CAD*, vol. 9, no. 2, pp. 3-5, February 1998.
- [74] S. Pendharkar and K. Shenai, "Performance Evaluation of High-Power GaAs Schottky and Silicon P-i-N Rectifiers in Hard- and Soft-Switching Applications," *IEEE Trans. Power Electronics*, vol. 13, no. 3, pp. 441-451, May 1998.
- [75] E. McShane, P. Khandelwal, A. Mulay, Y. Xu, and K. Shenai, "Systems on a Chip (SOC) CAD Tool Environment," *TCAD Driven CAD*, vol. 9, no. 5, pp. 5-6, May 1998.
- [76] P. Perugupalli, M. Trivedi, K. Shenai, and S. K. Leong, "Modeling and Characterization of an 80-V Silicon LDMOSFET for Emerging RFIC Applications," *IEEE Trans. Electron Devices*, vol. 45, no. 7, pp. 1468-1478, July 1998.
- [77] S. Pendharkar and K. Shenai, "Zero Voltage Switching Behavior of Punch-Through and Non Punch-Through IGBTs," *IEEE Trans. Electron Devices*, vol. 45, no. 8, pp. 1826-1835, August 1998.
- [78] M. Trivedi and K. Shenai, "Current Snap-Back and Negative Differential Resistance in Layered P-n-N Structures," *J. Appl. Phys.*, vol. 84, no. 4, pp. 2091-2098, August 1998.
- [79] C. Winterhalter, S. Pendharkar, and K. Shenai, "A Novel Circuit for Accurate Characterization and Modeling of the Reverse Recovery of High-Power High-Speed Rectifiers," *IEEE Trans. Power Electronics*, vol. 13, no. 5, pp. 924-931, September 1998.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [80] E. McShane, M. Trivedi, Y. Xu, P. Khandelwal, A. Mulay, and K. Shenai, "One-Chip Wonders," *IEEE Circuits and Devices Magazine*, vol. 14, no. 5, pp. 35-42, September 1998. **(invited paper)**.
- [81] S. Pendharkar, M. Trivedi, and K. Shenai, "Electrothermal Simulations in Punch-Through and Non Punch-Through IGBTs," *IEEE Trans. Electron Devices*, vol. 45, no. 10, pp. 2222-2231, October 1998.
- [82] M. Trivedi and K. Shenai, "IGBT Dynamics for Clamped Inductive Switching," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2537-2545, December 1998.
- [83] M. Trivedi and K. Shenai, "Failure Mechanisms of IGBTs Under Short Circuit and Clamped Inductive Switching Stress," *IEEE Trans. Power Electronics*, vol. 14, no. 1, pp. 108-116, January 1999.
- [84] P. Khandelwal, M. Trivedi, K. Shenai, and S. K. Leong, "Thermal and Package Performance Limitations in MOSFETs for RFIC Applications," *IEEE Trans. Microwave Theory and Techniques*, vol. 47, no. 5, pp. 575-585, May 1999.
- [85] M. Trivedi and K. Shenai, "Performance Evaluation of High-Power Wide Band-Gap Semiconductor Rectifiers," *J. Appl. Physics*, vol. 85, no. 9, pp. 6889-6897, May 1999.
- [86] M. Trivedi and K. Shenai, "Internal Dynamics of IGBT Under Zero-Voltage and Zero-Current Switching Conditions," *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1274-1282, June 1999.
- [87] M. Trivedi, P. Khandelwal, and K. Shenai, "Performance Modeling of RF Power MOSFETs," *IEEE Trans. Electron Devices*, vol. 46, no. 8, pp. 1794-1802, August 1999.
- [88] H. Morkoc R. Cingolani, W. Lambrecht, B. Gil, H. X. Jiang, J. Lin, D. Pavlidis, and K. Shenai "Material Properties of GaN in the Context of Electron Devices," *MRS Internet J. Nitride Semicond. Res.* 4S1, G1.2, 1999 **(invited paper)**.
- [89] M. Trivedi and K. Shenai, "Parasitic Extraction Methodology for Insulated Gate Bipolar Transistor," *IEEE Trans. Power Electronics*, vol., no. 4, pp. 799-804, July 2000.
- [90] M. Trivedi, P. Khandelwal, K. Shenai, and S. K. Leong, "Design and Modeling of Bulk and SOI LDMOSFETs for RF Wireless Applications," *Solid State Electronics*, vol. 44, pp. 1343-1354, August 2000.
- [91] K. Shenai, E. McShane, and S. K. Leong, "Lateral RF SOI Power MOSFETs with  $f_T$  of 6.9 GHz," *IEEE Electron Device Lett.*, vol. 21, no. 10, pp. 500-502, October, 2000
- [92] R. Vijayalakshmi, M. Trivedi, and K. Shenai, "Charge-Control Modeling of Power Bipolar Junction Transistors," *IEEE Trans. Power Electronics*, vol. 15, no. 6, pp 1072-1080, November 2000.
- [93] S. Azzopardi, C. Zardini, M. Trivedi, and K. Shenai, "Non-Destructive Extraction of Technological Parameter for Numerical Simulation of Conventional Planar Punch-Through IGBT," *Solid State Electron.*, Vol.44, No. 11, pp. 1899-1908, November, 2000.
- [94] K. Shenai, "Made-to-order Power Electronics," *IEEE Spectrum*, vol. 37, No. 7, pp. 50-55, July 2000 **(invited)**.
- [95] K. Shenai, "Power Semiconductor Manufacturer SOA Specifications Require Updating," *PCIM*, vol. 26, No. 12, pp. 26-32, December 2000 **(invited)**.
- [96] Trivedi, M. and Shenai, K., "Practical Limits of High-Voltage Thyristors on Wide Band-Gap Materials," *Journal of Applied Physics*, Volume 88, No.11, pp. 7313-7320, December, 2000.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [97] K. Shenai, "High-Power Robust Semiconductor Electronics Technologies in the New Millennium", *Microelectronics Journal*, Volume 32, Issues 5-6, pp. 397-408, 2001.
- [98] K. Shenai, P. G. Neudeck and G. Schwarze, "Design and Technology of Compact High-Power Converters," *IEEE Aerospace and Electronic Systems Magazine*, Vol. 16, Issue 3, pp. 27-31, March 2001 (**invited**).
- [99] E. McShane, M. Trivedi, and K. Shenai, "An Improved Approach to Application-Specific Power Electronics Education—Curriculum Development," *IEEE Trans. Education*, Volume 44, Issue 3, pp 282-288, August 2001.
- [100] E. McShane and K. Shenai, "The Design, Characterization, and Modeling of RF LDMOSFETs on Silicon-on-Insulator Material," *IEEE Trans. Electron Devices*, Volume 49, Issue 4, pp 643-651, April 2002.
- [101] M. Trivedi, E. McShane, R. Vijayalakshmi, A. Mulay, S. Abedinpour, S. Atkinson, and K. Shenai, "An Improved Approach to Application-Specific Power Electronics Education—Part II: Switch Characterization and Modeling," *IEEE Trans. Education*, Vol. 45, Issue 1, pp. 57-64, Feb. 2002.
- [102] Shenai, K., Trivedi, M., Neudeck, P.G., "Characterization of Hard-And-Soft Switching Performance of High-Voltage Si and 4H SiC PiN Diodes," *IEEE Trans. Electron Devices*, Volume 49, Issue 9, pp 1648-1656, September 2002.
- [103] S. Nigam, J. Kim, F. Ren, G. Chung, S. J. Pearton, J. R. William, K. Shenai, and P. Neudeck, "Effect of Contact Geometry on 4H-SiC Rectifiers with Junction Termination Extension," *Solid-State Electronics*, vol. 47, pp.57-60, 2003.
- [104] S. Nigam, J. Kim, F. Ren, G. Chung, S. J. Pearton, J. R. William, K. Shenai, and P. Neudeck, "Influence of Edge Termination Geometry on Performance of 4H-SiC p-i-n Rectifiers," *Solid-State Electronics*, vol. 47, pp.61-64, 2003.
- [105] S. Nigam, J. Hyun, B. Luo, F. Ren, G.Y. Chung, K. Shenai, P. G. Neudeck, S. J. Pearton and J. R. Williams, "Role of Device Area, Mesa Length and Metal Overlap Distance on Breakdown Voltage of 4H-SiC p-I-n Rectifiers," *Solid-State Electronics*, vol. 47, pp.1461-1464, 2003.
- [106] K. Shenai, K. F. Galloway, and R. D. Schrimpf, "The Effects of Space Radiation Exposure on Power MOSFETs: A Review," *Int. J. High Speed Electronics and Systems*, vol. 14, pp. 445-463, 2004 (**invited paper**).
- [107] K. Shenai and P. Boyapati, "A Novel Low-Power Soil Moisture Sensor," submitted to *IEEE J. Sensors* (2009).
- [108] K. Shenai and P. Boyapati, "Low-Power Sensor for Measuring Soil Electrical Conductivity," submitted to *IEEE Trans. Circuits and Systems* (2009).
- [109] K. Shenai and P. Boyapati, "A Novel Method of Wireless Communication in Soil and Water," submitted to *IEEE J. Solid-State Circuits* (2009).
- [110] K. Shenai, "A Novel Criteria for Screening of Power MOSFETs for Improving Field-reliability of Power Electronic Circuits," submitted to *IEEE Trans. Power Electronics* (2009).
- [111] K. Shenai, "An Improved Charge Pump Circuit," submitted to *IEEE J. Solid-State Circuits* (2009).

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

**Refereed Papers in International Conference Digests**

- [1] K. Shenai, K. Zaki, and R. W. Newcomb, "State Variable Equations for a Non-Linear Delay Circuit Model of IMPATT Diodes," in *Proc. Int. Symp. Microwaves and Communication*, 1981, pp.327-332.
- [2] K. Shenai and H. C. Lin, "Planar Etch Method for Enhanced Breakdown Voltages in Silicon Planar p-n Junctions," in *Ext. Abs. Spring Mtg. Electrochemical Society*, 1982, pp.295-296.
- [3] K. Shenai, "Avalanche Breakdown Voltages in Semiconductor Junctions," in *Ext. Abs. Spring Mtg. Electrochemical Society*, 1984, pp. 635-636.
- [4] K. Shenai and R. W. Dutton, "Characterization and Physics of Low-Field Electron Transport in GaAs MESFETs," in *Proc. Int. Symp. GaAs and Related Compounds*, vol. 83, 1986, pp.453-458.
- [5] K. Shenai, S. Al-Marayati, J. W. Kretchmer, and B. J. Baliga, "Characteristics of As-Deposited and Annealed Mo/LPCVD and Al/LPCVD W Contacts to Silicon," in *Proc. Tungsten and Other Refractory Metals for VLSI Applications III*, 1988, pp. 219-224.
- [6] K. Shenai, P. A. Piacente, G. A. Smith, N. Lewis, M. D. McConnell, and B. J. Baliga, "High-Temperature Stability of TiSi<sub>2</sub>/n Polysilicon/SiO<sub>2</sub> MOS Structures Formed by Conventional Thermal and Rapid Thermal Annealing," in *Proc. Tungsten and Other Refractory Metals for VLSI Applications III*, 1988, pp.333-338.
- [7] K. Shenai and B.J. Baliga, "Contact Resistance of Al + 1% Si and Mo/LPCVD W Metallizations to n- and p-Doped Si for Power Devices," in *Ext. Abs. Fall Mtg. Electrochemical Society*, 1988, pp. 1005-1006.
- [8] K. Shenai, P.A. Piacente, and B.J. Baliga, "Electrical Characteristics of TiSi<sub>2</sub>/n-Polysilicon/SiO<sub>2</sub>/Si MOS Capacitors Stressed Under High-Temperature Silicide Processing Conditions," in *Materials Research Soc. Symp. Proc.*, 1988, vol. 105, pp. 295-300.
- [9] K. Shenai, P. A. Piacente, G. A. Smith, N. Lewis, M. D. McConnell, J. F. Norton, E. L. Hall, and B. J. Baliga, "Degradation of TiSi<sub>2</sub>-Polysilicon Interfaces Due to High-Temperature Processing," in *Materials Research Soc. Symp. Proc.*, 1988, vol. 106, pp. 149-153.
- [10] K. Shenai, "Characterization and Physics of Threshold Voltage Dependence on Defect Related Properties of Channel-Buffer (Substrate) Interfaces in GaAs MESFETs Fabricated by MBE," in *Materials Research Soc. Symp. Proc.*, 1988, vol. 102, pp. 191-195.
- [11] C. S. Korman, K. Ngo, A. Yerman, G. Claydon, J. Walden, K. Shenai, M. Kuo, B. J. Baliga, and W. Tantraporn, "A Synchronous Rectifier for High-Density Power Supplies," in *Tech. Dig. Int. High Frequency Power Conversion (HFPC)*, 1988, pp. 128-139.
- [12] K. Shenai, P. A. Piacente, N. Lewis, M. D. McConnell, G. A. Smith, and B. J. Baliga, "On the Adhesion of WSi<sub>2</sub> to Doped and Undoped Polysilicon," in *Materials Research Soc. Symp. Proc.*, 1988, vol. 119, pp. 177-182.
- [13] K. Shenai, N. Lewis, E. L. Hall, G. A. Smith, M. D. McConnell, P. A. Piacente, and B. J. Baliga, "Thermodynamics of the Surface Stability of TiSi<sub>2</sub> on Doped and Undoped Polysilicon at Elevated Temperatures for Electronic Applications," in *Ext. Abs. Spring Mtg. Electrochemical Society*, 1988, vol.88-1, p. 439.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [14] K. Shenai, S. Al-Marayati, R. Saia, N. Lewis, G. A. Smith, and B. J. Baliga, "The Effect of RIE in  $\text{CHF}_3/\text{CO}_2$  Plasma and Successive Residual Silicon Damage Removal on the Contact Resistance of Al-nSi and Alusil-nSi Contacts," in *Proc. Symp. Plasma Processing*, 1988, vol. 88-22, pp.179-193
- [15] K. Shenai, P. A. Piacente, G. A. Smith, N. Lewis, M. D. McConnell, and B. J. Baliga, "The Formation and Properties of Rapid Thermally Annealed (RTA)  $\text{TiSi}_2$  on Doped and Undoped Polysilicon," in *Ext. Abs Spring Mtg. Electrochemical Society*, 1988, vol. 88-1, pp. 129-130.
- [16] K. Shenai, P. A. Piacente, and B. J. Baliga, "Reliable Low Resistance Al-TiW- $\text{TiSi}_2$ -nSi Contacts for Silicon VLSI and Smart-Power™ Applications," in *Proc. Int. Symp. Advanced Materials for ULSI*, 1988, vol. 88-19, pp. 155-164.
- [17] N. Lewis, K. Shenai, and E. L. Hall, "TEM Analysis of  $\text{TiSi}_2$  on Si and Polysilicon," in *Proc. Ann. Mtg. Electron Microscopy Soc. of America*, 1988, pp. 886-887.
- [18] S. Al-Marayati, K. Shenai, N. Lewis, and B.J. Baliga, "Defect Engineering and the Contact Resistance of Shallow and Deep Junctions in Silicon Discrete and Integrated Power Devices," in *Ext. Abs. Fall Mtg. Electrochemical Society*, 1988, vol. 88-2, pp.638-639.
- [19] K. Shenai, P. A. Piacente, R. Saia, W. Hennessy, C. S. Korman, and B. J. Baliga "A Novel High-Frequency Power FET Structure Fabricated using LPCVD  $\text{WSi}_2$  Gate and LPCVD W Source Contact Technology," in *IEEE IEDM Tech. Dig.*, 1988, pp. 804-808.
- [20] K. Shenai, P. A. Piacente, S. Al-Marayati, R. Saia, and B. J. Baliga, "Extremely Low Resistance and Reliable Al-TiW- $\text{TiSi}_2$  Contacts to n+ and p+-Si for Silicon VLSI and Smart-Power™ Applications," in *Ext. Abs. Fall Mtg. Electrochemical Society*, 1988, vol. 88-2, pp. 359-360. Also published in the Symp. Proceedings, 1989.
- [21] K. Shenai, P. A. Piacente, S. Al-Marayati, and B. J. Baliga, "Characteristics of Al- $\text{TiSi}_2$  Contacts to n+ and p+ Silicon," in *Ext. Abs. Fall Mtg. Electrochemical Society*, 1988, vol. 88-2, pp. 461-462. Also published in Symp. Proceedings, 1989.
- [22] K. Shenai, W. Hennessy, R. Saia, N. Lewis, G. A. Smith, and B. J. Baliga, "Effect of Ion Bombardment on the Dopant Diffusion During the Reactive Ion Etching of Dielectric Films Deposited on Silicon," in *Proc. Symp. Processing and Characterization of Materials Using Ion Beams*, 1989, vol. 128, pp. 731-736.
- [23] N. Lewis, K. Shenai, P. A. Piacente, and B.J. Baliga, "Effect of Doping on the Grain Structure of As-Deposited and High-Temperature Annealed  $\text{WSi}_2$  Films on Polysilicon," in *Proc. Symp. High Resolution Microscopy of Materials*, 1989, vol. 138, pp. 421-426.
- [24] W. Hennessy, K. Shenai, T. B. Gorczyca, and R. Saia, "Evaluation of LPCVD W Technology for Gate-Source Strapping of High-Density Large-Area Power MOSFETs," in *Proc. Tungsten and Other Refractory Metals for VLSI Applications IV*, 1989, pp. 101-110.
- [25] K. Shenai, W. Hennessy, T. B. Gorczyca, B. Gorowitz, R. Saia, C. S. Korman, and B. J. Baliga, "A Novel High-Frequency Power FET Structure Fabricated Using LPCVD Tungsten Based Spacer Technology," in *Proc. Tungsten and Other Refractory Metals for VLSI Applications IV*, 1989, pp. 121-128.
- [26] K. Shenai, P. A. Piacente, N. Lewis, G. A. Smith, M. D. McConnell, and B. J. Baliga, "Effect of Silicide Deposition and Annealing Conditions on LPCVD  $\text{WSi}_2$ /Polysilicon/ $\text{SiO}_2$

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- MOS Capacitors,” in *Proc. Tungsten and Other Refractory Metals for VLSI Applications IV*, 1989, pp. 333-341.
- [27] K. Shenai, P. A. Piacente, N. Lewis, G. A. Smith, M. D. McConnell, D. W. Skelly, J. F. Norton, and B. J. Baliga, “Optical Characteristics of As-Deposited and High Temperature Annealed  $\text{WSi}_2$  Films Deposited on Doped and Undoped Polysilicon,” in *Ext. Abs. Spring Mtg. Electrochemical Society*, 1989, p. 325.
- [28] K. Shenai, R. S. Scott, and B. J. Baliga, “New Material and Device Design Considerations for High-Power Electronic Applications,” in *Proc. Amorphous and Crystalline Silicon Carbide II - Recent Developments*, 1989, pp. 135-142.
- [29] K. Shenai, C. S. Korman, J. P. Walden, A. J. Yerman, and B. J. Baliga, “Optimized Silicon Low-Voltage Power MOSFETs for High-Frequency Power Conversion,” in *IEEE Power Electronics Specialists Conf. (PESC) Rec.*, 1989, vol. 1, pp. 180-189.
- [30] R. A. Fisher, C. S. Korman, G. A. Franz, G.W. Ludwig, J. P. Walden, S. A. El-Hamamsy, K. Shenai, and M. Kuo,”Performance of Low Loss Synchronous Rectifiers in a Series-Parallel Resonant dc-dc Converter,” in *Proc. IEEE Applied Power Electronics Conf. (APEC)*, 1989, pp. 240-246.
- [31] K. Shenai, N. Lewis, G. A. Smith, and B. Cohen, “Transient Thermal Effect Arising from Substrate Thickness Variations on  $\text{TiSi}_2$  Film Properties and its Compensation Using a Closed Loop Temperature Control Mechanism of a Rapid Thermal Processor,” in *Proc. Int. Symp. ULSI Science and Technology*, 1989, vol. 89-9, pp.162-172.
- [32] K. Shenai, N. Lewis, and G. A. Smith, “Effect of Ion Implantation Parameters on the Film Properties of Furnace Annealed and Rapid Thermally Annealed  $\text{TiSi}_2$  Films Formed on Heavily Doped Silicon,” in *Proc. Int. Symp. ULSI Science and Technology*, 1989, vol. 89-9, pp. 173-183.
- [33] K. Shenai and B. J. Baliga, “Refractory Silicide Technologies for Smart-Power™ Applications,” in *Ext. Abs. Spring Mtg. Electrochemical Society*, 1989, pp. 443-444. Also published in Symp. Proceedings, 1989.
- [34] K. Shenai and B. J. Baliga, “Diamond: A Semiconductor for High-Temperature, High-Power Electronics,” in *Ext. Abs. Spring Mtg. Electrochemical Society*, 1989, pp. 156-157. Also published in Symp. Proceedings, 1989.
- [35] K. Shenai, C. S. Korman, and B. J. Baliga, “Optimum Silicon and GaAs Power Field-Effect Transistors for Advanced High-Density, High-Frequency Power Supply Applications,” in *Tech. Dig Int. High Frequency Power Conversion (HFPC)*, 1989, pp.32-61.
- [36] K. Shenai, G. A. Franz, S. Paul, and S. Haque-Ahmed, “A Novel Circuit Simulation Model of Large Area Power MOSFETs Suitable for High-Frequency Power Switching Applications,” in *Tech. Dig. Int. High Frequency Power Conversion (HFPC)*, 1989, pp.331-356.
- [37] K. Shenai, “Technology Trends in High-Frequency Power Semiconductor Discrete Devices and Integrated Circuits,” in *Tech. Dig. Int. High Frequency Power Conversion (HFPC)*, 1989, pp. 1-23.
- [38] K. Shenai, C. S. Korman, J. P. Walden, A. J. Yerman, and B. J. Baliga, “Optimized Silicon Low-Voltage Power MOSFETs for High-Frequency Power Conversion,” in *IEEE Power Electronics Specialists Conf. (PESC) Rec.*, 1989, vol. 1, pp. 180-189.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [39] C. S. Korman, K. Shenai, H. R. Chang, and J.P. Walden, "High Performance Power DMOSFET with Integral Schottky Diode," in *IEEE Power Electronics Specialists Conf. (PESC) Rec.*, 1989, vol. 1, pp.176-179.
- [40] K. Shenai, N. Lewis, G. A. Smith, and M. D. McConnell, "On the Reactive Ion Etching of Dielectric Layers Deposited/formed on LPCVD WSi<sub>2</sub> Films," in *Proc. Tungsten and Other Advanced Metals for VLSI/ULSI Applications V*, 1990, pp. 415-422.
- [41] K. Shenai, N. Lewis, and M. Burrell, "Physical Mechanisms Related to the Degradation of LPCVD Tungsten Contacts at Elevated Temperatures," in *Proc. Tungsten and Other Advanced Metals for VLSI/ULSI Applications V*, 1990, pp. 317-324.
- [42] K. Shenai, "Accurate Characterization of Gate Resistance and Its Effect on High-Frequency Switching Efficiencies of Power MOSFETs," in *IEEE Power Electronics Specialists Conf. (PESC) Rec.*, 1990, vol. 1, pp. 107-112.
- [43] K. Shenai, W. Hennessy, M. Ghezzi, C. Korman, H. Chang, V. Temple, and M. S. Adler, "Optimum Low-Voltage Silicon Power MOSFETs Fabricated Using Scaled Trench Technologies," in *IEEE IEDM Tech. Dig.*, 1990, pp. 793-797.
- [44] R. S. Wrathall, B. J. Baliga, K. Shenai, W. Hennessy, and T. P. Chow, "Charge Controlled 80-V Lateral DMOSFET with Very Low Specific On-Resistance Designed for an Integrated Power Process," in *IEEE IEDM Tech. Dig.*, 1990, pp. 954-957.
- [45] K. Shenai, "A Study of Furnace and Rapid Thermally Annealed LPCVD WSi<sub>2</sub> Films on Mono- and Polycrystalline Silicon," in *Proc. Tungsten and Other Advanced Metals for ULSI Applications VII*, 1991.
- [46] K. Shenai, "Optimized LPCVD WSi<sub>2</sub> Contacts and Interconnects for ULSI Multilevel Metallization Applications," in *Proc. Tungsten and Other Advanced Metals for ULSI Applications VII*, 1991.
- [47] K. Shenai, W. Hennessy, R. Saia, and M. Ghezzi, "A Novel Trench Planarization Technique using Polysilicon Refill, Polysilicon Oxidation, and Oxide Etchback," in *Proc. IEEE Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, 1991, p. 198.
- [48] K. Shenai, "Effect of Scaling on High-Frequency Switching Efficiencies of Power MOSFETs," in *Proc. IEEE Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, 1991, p.83.
- [49] K. Shenai, "Power Semiconductors: Status and Trends in Process/Device/Circuit CAD," in *Tech. Dig. Symp. Semiconductor Modeling and Simulation*, 1993, p. 21 (**invited paper**).
- [50] K. Shenai, "Emerging Power Semiconductor Device Technologies," in *Proc. Workshop Custom Design of Application-Specific Power Semiconductor Devices and Circuits*, 1994 (**invited paper**).
- [51] I. Widjaja, A. Kurnia, D. Divan, and K. Shenai, "Computer Simulation and Design Optimization of IGBTs in Soft-Switching Converters," in *Proc. IEEE Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, 1994, pp. 105-109.
- [52] K. Shenai, D. Hodge, M. D. Feuer and J. Cunningham, "Novel Ultralow R<sub>on</sub> MBE GaAs MOSFETs for High-Frequency High-Temperature Switched-Mode Power Converter Applications," in *Proc. Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, 1994, pp. 149-153.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [53] I. Widjaja, A. Kurnia, D. Divan, and K. Shenai, "Conductivity Modulation Lag During IGBT Turn on in Resonant Converter Applications," in *Dig. IEEE Ann. Device Research Conf (DRC)*, 1994, pp. 35-36.
- [54] K. Shenai, "Prospects of Wide Energy Band gap Semiconductors for High-Power Optoelectronics," in *Proc. Conf. Emerging Optoelectronic Technologies (CEOT)*, 1994, pp. 190-194 (**invited paper**).
- [55] K. Shenai, "Optically Triggered High-Power Semiconductor Devices," in *Proc. Conf. Emerging Optoelectronic Technologies (CEOT)*, 1994, pp. 237-242 (**invited paper**).
- [56] K. Shenai, R. Manukonda, and H. Vyas, "Semiconductor Process and Technology Integration Strategies for Rapid Product Development Cycles," in *Proc. Conf. Emerging Optoelectronic Technologies (CEOT)*, 1994, pp. 134-136 (**invited paper**).
- [57] K. Shenai, "A Fully Integrated CAD Infrastructure for the Design, Optimization, and Virtual Manufacturing of Discrete and Integrable Power Semiconductor Devices and Circuits," in *Proc. IEEE PELS Workshop on Computers in Power Electronics*, 1994, pp.6-10 (**invited paper**).
- [58] K. Shenai, "Mixed-mode circuit simulation: An emerging CAD tool for the design and optimization of power semiconductor devices and circuits," in *Proc. IEEE PELS Workshop on Computers in Power Electronics*, 1994, pp. 1-5 (**invited paper**).
- [59] I. Widjaja, A. Kurnia, D. Divan, and K. Shenai, "Dynamics of Punch-Through and Non Punch-Through IGBT Turn On Mechanism in Resonant Converters," in *Dig. European Solid State Device Research Conf. (ESSDERC)*, 1994.
- [60] H. H. Li, I. Widjaja, A. Kurnia, D. Divan, and K. Shenai, "The Effect of Bipolar Transistor in the Switching Dynamics of IGBTs in Resonant Converter Applications," in *IEEE BCTM Tech. Dig.*, 1994, pp. 135-138. (**won Best Paper Award**)
- [61] D. Dallmann and K. Shenai, "Evaluation of Self-Heating Effects in Bulk and SOI CMOS ULSI," in *Int. Integrated Reliability Workshop Final Rep.*, 1994, pp. 83-89.
- [62] E. Rosenbaum and K. Shenai, "Reliability Modeling and Simulation Discussion Group," in *Int. Integrated Reliability Workshop Final Rep.*, 1994, p. 143.
- [63] K. Shenai, "Low-Power, High-Speed Deep Submicron VLSI: Device Technologies and Interconnect Modeling Issues," in *Proc. Int. Symp. Microelectronics*, 1994, pp. 1-3 (**invited paper**).
- [64] K. Shenai, "Thermal Effects in Integrable Power Semiconductor Devices," in *Proc. Int. Symp. Microelectronics*, 1994, pp. 138-143.
- [65] D. Dallmann and K. Shenai, "Investigation of Self-Heating Effects Submicron SOI MOSFETs," in *Proc. Int. Symp. Microelectronics*, 1994, pp. 625-630.
- [66] J. H. Booske, L. Zhan, R. F. Cooper, J. L. Shohet, K. Shenai, D. Dallman, M. J. Goeckner, R. Breun, W. N. G. Hitchon, E. Wickesberg, R. Speth, J. R. Jacobs, and G. Was, "Buried Ceramic Layer Formation in Glass and Silicon Using Plasma Source Ion Implantation," in *IEEE Int. Conf. Plasma Science – 1994 Conf. Record*, p. 166.
- [67] M. Trivedi, C. Winterhalter, H. H. Li, and K. Shenai, "Performance Evaluation of an Emitter-Switched Thyristor for Resonant Converter Applications," in *Proc. IEEE Int. Conf. Power Electronics and Drive Systems (PEDS)*, 1995, pp. 13-15 (**invited paper**).

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [68] K. Fischer and K. Shenai, "The Effect of Parasitic Bipolar Transistor on the Performance and Reliability of Scaled Vertical Power DMOSFETs," in *Proc. IEEE Int. Conf. Power Electronics and Drive Systems (PEDS)*, 1995, pp. 251-255.
- [69] N. Krasnoperov and K. Shenai, "Performance and Reliability Comparison of Power DMOSFET Structures with and without an Integral Schottky Diode," in *Proc. IEEE Int. Conf. Power Electronics and Drive Systems (PEDS)*, 1995, pp. 276-277.
- [70] H. H. Li, A. Kurnia, D. Divan, and K. Shenai, "High-Temperature Turn-Off Performance of IGBTs in Resonant Converters," in *Proc. IEEE Int. Conf. Power Electronics and Drive Systems (PEDS)*, 1995, pp. 256-258.
- [71] H. H. Li, A. Kutkut, H. Wiegman, A. Kurnia, D. Divan, and K. Shenai, "High-Temperature Characteristics of IGBTs in Soft- and Hard-Switching Converters," in *Proc. IEEE Applied Power Electronics Conf. (APEC)*, pp. 733-735, 1995.
- [72] H. H. Li, M. Trivedi, S. Pendharkar, C. Winterhalter, and K. Shenai, "Performance Comparison of IGBTs and MCTs in Resonant Converters," in *IEEE Power Electronics Specialists Conf. (PESC) Rec.*, 1995, pp. 50-54.
- [73] C. Winterhalter, S. Pendharkar, and K. Shenai, "Modeling and Characterization of Reverse Recovery Performance of High-Power GaAs Schottky and Silicon P-i-N Rectifiers," in *IEEE Power Electronics Specialists Conf. (PESC) Rec.*, 1995, pp. 847-850.
- [74] S. Pendharkar and K. Shenai, "A Critique of the Turn-On Physics of Power Bipolar Devices," in *IEEE BCTM Tech. Dig.*, 1995, pp. 209-212.
- [75] H. H. Li and K. Shenai, "Simulation Prototyping of High-Power Modules," in *IEEE BCTM Tech. Dig.*, 1995, pp. 213-216.
- [76] H. H. Li, M. Trivedi, and K. Shenai, "Dynamics of IGBT Performance in Hard- and Soft-Switching Converters," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1995, pp. 1006-1009.
- [77] S. Pendharkar, C. Winterhalter, M. Trivedi, H. H. Li, A. Kurnia, D. Divan, and K. Shenai, "Test Circuits for Verification of Power Device Models," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1995, pp. 1055-1060.
- [78] K. Fischer and K. Shenai, "Synchronous Rectifier as a Test Circuit for High-Frequency Power MOSFET Model Verification," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1995, pp. 1091-1097.
- [79] H. H. Li, H. Wiegman, N. Kutkut, A. Kurnia, D. Divan, and K. Shenai, "High-Temperature Characteristics of IGBTs in Soft- and Hard-Switching Converters," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1995, pp. 733-735.
- [80] M. Trivedi, C. Winterhalter, H. H. Li, and K. Shenai, "Performance Evaluation of an Emitter-Switched Thyristor for Resonant Converter Applications," in *Proc. 1995 Int. Conf. Power Electronics and Drive Systems*, pp. 13-15, 1995.
- [81] N. Krasnoperov and K. Shenai, "Performance and Reliability Comparison of Power DMOSFET Structures with and without an Integral Schottky Diode," in *Proc. 1995 Int. Conf. Power Electronics and Drive Systems*, pp. 276-280, 1995.
- [82] K. Fischer and K. Shenai, "the Effect of Parasitic Bipolar Transistor on the Performance and Reliability of Scaled Vertical Power DMOSFETs," in *Proc. 1995 Int. Conf. Power Electronics and Drive Systems*, pp. 251-255, 1995.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [83] M. Trivedi, H. H. Li, S. Pendharkar, and K. Shenai, "Application of IGBT, MCT, and EST in Hard- and Soft-Switching Power Converters," in *Proc. IEEE Power Electronics, Drives and Energy Systems (PEDES) Conf.*, 1996, pp. 201-205.
- [84] S. Pendharkar and K. Shenai, "High Temperature Performance of High-Power GaAs Schottky and Silicon P-i-N Rectifiers in Hard and Soft-Switching Power Converters," in *Dig. Power Electronics and Industrial Drives Conf.*, 1996.
- [85] S. Pendharkar and K. Shenai, "Performance Evaluation of High-Power GaAs Schottky and Silicon P-i-N Rectifiers in Hard- and Soft-Switching Applications," in *Proc. IEEE Applied Power Electronics Conf. (APEC)*, 1996, pp. 234-238.
- [86] S. Pendharkar and K. Shenai, "A Circuit Simulation Model for High-Power High-Speed GaAs Schottky Diodes," in *Proc. IEEE Applied Power Electronics Conf. (APEC)*, 1996, pp.246-249.
- [87] K. Fischer and K. Shenai, "Ultra-High Performance Rugged Scaled Power MOSFETs for High-Frequency Power Conversion," in *Proc. IEEE Applied Power Electronics Conf.(APEC)*, 1996, pp. 270-275.
- [88] K. Shenai, C. Q. Lee, and I. Bataarseh, "An Integrated Power Electronics Curriculum," in *Dig. NSF Workshop on Power Electronics*, 1996, pp. 21-26.
- [89] K. Shenai, "Application-Specific Power Electronic Modules (ASPEMs): Technologies and Challenges," in *Proc. Power Systems*, 1996 (**invited paper**).
- [90] M. Trivedi and K. Shenai, "Internal Dynamics of IGBT During Short Circuit Switching," in *IEEE BCTM Tech. Dig.*, 1996, pp. 77-80.
- [91] M. Trivedi and K. Shenai, "High-Power Solid-State Devices and Smart-Power ICs," in *Proc. Int. Electron Devices and Materials Symp. (IEDMS)*, 1996, pp. A3-6—A3-9.(invited paper).
- [92] M. Trivedi and K. Shenai, "Modeling IGBT Turn-Off in Hard- and Soft-Switching Power Converters," in *Proc. IEEE Applied Power Electronics Conf. (APEC)*, 1997, pp.156-160.
- [93] P. Perugupalli, M. Trivedi, K. Shenai, and S. K. Leong, "Modeling and Characterization of 80-V LDMOSFET for RF Communications," in *IEEE BCTM Tech. Dig.*, 1997, pp. 92-95.
- [94] M. Trivedi and K. Shenai, "Trade-Off in IGBT Safe Operating Area and Performance Parameters," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1997, pp. 949-954.
- [95] M. Trivedi, K. Shenai and E. Larson, "Critical Evaluation of IGBT Performance in Zero Current Switching Environment," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1997, pp. 989-993.
- [96] E. McShane and K. Shenai, "Functionally Integrated System on a Chip: Technologies, Architectures, CAD Tools, and Applications," in *Proc. Int. Workshop Innovative Architectures for Future Generation High-Performance Processors and Systems*, 1997, pp. 67-75.
- [97] P. Perugupalli, M. Trivedi, K. Shenai, and S. K. Leong, "Performance Evaluation of Bulk Si and SOI RF LDMOSFETs for Emerging RFIC Applications," in *Dig. IEEE SOI Conf.*, 1997, pp.108-109.
- [98] M. Trivedi and K. Shenai, "Characterization, Modeling, and Optimization of High Power Module Packaging," in *Proc. IEEE Electrical Performance and Electronic Packaging (EPEP)*, 1997, pp. 103-106.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [99] M. Trivedi and K. Shenai, "Hybrid GaN/SiC High Power Rectifiers for Improved Switching Characteristics," in *Dig. Int. Conf. Nitride Semiconductors (ICNS)*, 1997.
- [100] K. Shenai, E. McShane, and M. Trivedi, "Electronics Technologies for Intelligent Transportation Systems," in *Dig. IEEE Conf. Intelligent Transportation Systems (ITSC)*, 1997, pp.302-307. (Available only as a CD-ROM).
- [101] K. Shenai, "Thermally Engineered High-Power Wide Bandgap Material Technologies," in *Materials Research Soc. Symp.Proc.*, 1997 (**invited paper**).
- [102] M. Trivedi and K. Shenai, "Mixed-Mode Simulation for Power System Optimization," in *Proc. IEEE Int. Conf. Microelectronics (MIEL)*, 1997, pp. 451-457.
- [103] M. Trivedi and K. Shenai, "IGBT Dynamics for Short-Circuit and Clamped Inductive Switching," in *Proc. IEEE Applied Power Electronics Conf. (APEC)*, 1998, pp. 743-748.
- [104] P. Perugupalli, M. Trivedi, K. Shenai, and S. K. Leong, "High Temperature Performance of LDMOSFETs Used in RFIC Applications," in *Proc. Engineering Foundation Conf. High Temperature Electronic Materials, Devices, and Sensors (HTEM)*, 1998, pp.100-104.
- [105] M. Trivedi and K. Shenai, "High Temperature Performance of Hybrid GaN/SiC High Power Diodes," in *Proc. Engineering Foundation Conf. High Temperature Electronic Materials, Devices, and Sensors (HTEM)*, 1998, pp. 117-122.
- [106] E. McShane, K. Shenai, L. Alkalai, E. Kolawa, and E. Holmberg, "Monolithic Microprocessor and RF Transceiver for Low-Power Mobile Applications," in *SPIE Aerospace/Defense Sensing and Controls Conf. (AeroSense)*, 1998, vol. 3366, pp. 20-28.
- [107] P. Perugupalli, Y. Xu, and K. Shenai, "Measurement of Thermal and Packaging Limitations in LDMOSFETs for RFIC Applications," in *Proc. IEEE Instrumentation and Measurement Technology Conf. (IMTC)*, 1998, pp. 160-164.
- [108] M. Trivedi, R. Evazians, and K. Shenai, "A Novel Base Drive Circuit for Accurate Measurement and Modeling of High-Speed Power Bipolar Transistors," in *Proc. IEEE Instrumentation and Measurement Technology Conf. (IMTC)*, 1998, pp.511-514.
- [109] M. Trivedi, R. Evazians, and K. Shenai, "Test Circuits for Characterizing Power Transistors in ZVS and ZCS Circuits," in *Proc. IEEE Instrumentation and Measurement Technology Conf. (IMTC)*, 1998, pp. 515-518.
- [110] M. Trivedi and K. Shenai, "Thermal Limitations Due to Semiconductor and Packaging in High Power Switches," in *Proc. IEEE Instrumentation and Measurement Technology Conf.(IMTC)*, 1998, pp. 618-621.
- [111] M. Trivedi and K. Shenai, "Turn-Off Failure of IGBTs Under Clamped Inductive Load," in *IEEE Power Electronic Specialists Conf. (PESC) Rec.*, 1998, pp. 1191-1195.
- [112] M. Trivedi, R. Vijayalakshmi, K. Shenai, and B. Hesterman, "Improved Capacitance Model for Power Bipolar Transistor Turn-Off Performance," in *IEEE Power Electronics Specialists Conf.(PESC) Rec.*, 1998, pp. 1214-1218.
- [113] K. Shenai, E. McShane, A. Johnson, and T. DeFanti, "Advanced Electronic Visualization and Virtual Reality Technologies for Education and Research Training," in *Proc. IASTED Int. Conf. Computers and Advanced Technology in Education (CATE)*, 1998, pp.3-6.
- [114] M. Trivedi and K. Shenai, "Prospect of Soft-Switching Power Converter Technologies," in *Proc. Int. Power Modulator Symp. (IPMS)*, 1998, pp. 119-122.
- [115] P. Khandelwal, M. Trivedi, and K. Shenai, "Thermal Issues in LDMOSFET Packages," in *Dig. European Solid-State Device Research Conf. (ESSDERC)*, 1998.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [116] K. Shenai and E. McShane, "SOI Device and Technology Modeling for Ultra Low-Power and High Power Electronics," in *Dig. US-Mexico Workshop Semiconductor Device Modeling and Characterization*, 1998, pp. 7-13.
- [117] E. McShane, M. Trivedi, and K. Shenai, "Technologies and CAD Requirements of Ultra Low-Power Electronics," in *Dig. US-Mexico Workshop Semiconductor Device Modeling and Characterization*, 1998, pp. 25-28.
- [118] M. Trivedi and K. Shenai, "MOS and Bipolar Semiconductor Device Characterization and Modeling," in *Dig. US-Mexico Workshop Semiconductor Device Modeling and Characterization*, 1998, pp. 29-32.
- [119] M. Trivedi and K. Shenai, "Framework for Power Package Design and Optimization," in *Proc. IEEE Int. Workshop Integrated Power Packaging (IWIPP)*, 1998, pp. 35-38.
- [120] A. Mulay and K. Shenai, "IGBT Module Characterization, Modeling, and Parasitic Extraction," in *Proc. IEEE Int. Workshop Integrated Power Packaging (IWIPP)*, 1998, pp. 62-65.
- [121] K. Shenai and M. Trivedi, "IGBT Evaluation for Hard- and Soft-Switching Applications," in *Dig. PEBB Soft Switching Workshop (SSW)*, 1998.
- [122] A. Mulay, M. Trivedi, and K. Shenai, "Dynamic Avalanching Considerations in Optimization of Reverse Conducting Diode in IGBT Modules," in *IEEE BCTM Tech. Dig.*, 1998, pp. 195-198.
- [123] M. Trivedi and K. Shenai, "Power Semiconductor Devices for Mega-Watt Power Switching," in *IEEE Dig. High Voltage Workshop (HVW), Power Module*, 1998.
- [124] A. Mulay, M. Trivedi, and K. Shenai, "Impact of Dynamic Avalanching of Reverse Conducting Diode in IGBT Module on Optimum Power Converter Design," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1998, pp. 848-852.
- [125] R. Vijayalakshmi, M. Trivedi, and K. Shenai, "Power Bipolar Transistor Performance in Hard- and Soft-Switching Power Converters," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1998, pp. 888-892.
- [126] M. Trivedi and K. Shenai, "High Temperature Capability of Devices on Si and Wide Band-Gap Materials," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1998, pp. 959-962.
- [127] M. Trivedi, S. Pendharkar, and K. Shenai, "High Temperature Performance Limits of IGBT Modules," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1998, pp. 977-981.
- [128] R. Vijayalakshmi, M. Trivedi, and K. Shenai, "Improved Charge Control Models of Power Bipolar Transistors," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1998, pp. 1011-1015.
- [129] A. Mulay, M. Trivedi, R. Vijayalakshmi, and K. Shenai, "Switching Dynamics of Power Bipolar Transistors in High Frequency Electronic Ballast," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1998, pp. 2130-2136.
- [130] E. McShane, K. Shenai, L. Alkalai, E. Kolawa, V. Boyadzhyan, B. Blaes, and W. C. Fang, "Novel Design for Testability of a Mixed-Signal VLSI IC," in *Proc. Great Lakes Symp. VLSI (GLSVLSI)*, 1999, pp. 97-100.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [131] E. McShane, K. Shenai, L. Alkalai, E. Kolawa, V. Boyadzhyan, B. Blaes, and W. C. Fang, "Monolithic Microprocessor and RF Transceiver in 0.25-micron FDSOI CMOS," in *Proc. Great Lakes Symp. VLSI (GLSVLSI)*, 1999, pp. 332-333.
- [132] E. McShane, K. Shenai, L. Alkalai, E. Kolawa and E. Holmberg, "Monolithic Microprocessor and RF Transceiver for Low-Power Mobile Applications," in *SPIE Proc. Robotic and Semi-Robotic Ground Vehicle Technology*, Edited by Grant R. Gerhart and Ben A. Abbott, Vol. 3366, Paper # 3366-05, pp. 20-28, ISBN: 0-8194-2815-9, August 1998.
- [133] R. Vijayalakshmi and K. Shenai, "Characterization and Physical Modeling of Power Bipolar Transistors in Soft Switching Converters," in *Proc. IEEE Applied Power Electronics Conf. (APEC)*, 1999, pp. 670-675.
- [134] S. Azzopardi, C. Zardini, M. Trivedi, and K. Shenai, "A Punch-Through IGBT Model Using a Simple Technological Parameters Extraction Method for Two-Dimensional Physical Simulation," in *Proc. European Power Electronics (EPE) Conf.*, 1999.
- [135] E. McShane, K. Shenai, T. DeFanti, and A. Johnson, "Education and Manufacturing in the Next Millennium," in *Proc. Conf. Space Manufacturing, High Frontier Conf.*, 1999, pp.186-189.
- [136] E. McShane, N. Keskar, and K. Shenai, "Space Electronics Technologies for the Next Millennium," in *Proc. Conf. Space Manufacturing, High Frontier Conf.*, 1999, pp. 297-300.
- [137] E. McShane, A. Mulay, S. Abedinpour, R. Vijayalakshmi, M. Trivedi, and K. Shenai, "University-Industry Cooperative Laboratory Development for Design and Characterization of Robust Power Converters," in *Proc. IEEE Biennial University-Government-Industry Microelectronics Symp. (UGIM)*, 1999.
- [138] E. McShane and K. Shenai, "University-Industry Cooperative Laboratory Development for an RF IC and Mixed-Signal VLSI Graduate/Undergraduate Curriculum," in *Proc. IEEE Biennial University-Government-Industry Microelectronics Symp. (UGIM)*, 1999.
- [139] E. McShane, K. Shenai, T. DeFanti, and A. Johnson, "National Testbed for Microelectronics Education and Research Training," in *Proc. IEEE Biennial University-Government-Industry Microelectronics Symp. (UGIM)*, 1999.
- [140] P. Khandelwal, K. Chinnaswamy, and K. Shenai, "RF Package Characterization and Modeling," in *Proc. IEEE Biennial University-Government-Industry Microelectronics Symp. (UGIM)*, 1999, pp. 182-185.
- [141] M. Trivedi and K. Shenai, "Recent Advances and Issues in Resonant Power Conversion," in *Proc. IEEE Industrial Electronics Conf. (IECON)*, 1999.
- [142] M. Trivedi and K. Shenai, "Physical Analysis of Current Snap-Back Phenomenon in Buffered High-Power Rectifiers," in *IEEE BCTM Tech. Dig.*, 1999, pp. 80-83.
- [143] K. Shenai and E. McShane, "Electronics for High-Energy Physics Experiment in Integration Era," in *Proc. Workshop Electronics for the LHC Experiments*, 1999, pp. 14-22 (**invited keynote paper**).
- [144] N. Keskar, K. Shenai, and P. Neudeck, "Transient Characterization of SiC *pn* Diode," in *Proc. Int. SiC and Related Materials Conf. (ICSCRM)*, 1999.
- [145] N. Keskar, K. Shenai, and P. Neudeck, "Defect Modeling and Simulation of 4H SiC *pn* Diode," in *Proc. Int. SiC and Related Materials Conf. (ICSCRM)*, 1999.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [146] M. Trivedi and K. Shenai, "Comparison of RF Performance of Vertical and Lateral DMOSFET," in *Proc. IEEE Int. Symp. Power Semiconductor Devices and ICs (ISPSD)*, 1999, pp. 245-248.
- [147] N. Keskar, M. Trivedi, and K. Shenai, "Device Reliability and Robust Power Converter Development," in *Proc. European Symp. Reliability of Electron Devices, Failure Physics and Analysis (ESREF)*, 1999, pp. 1121-1130.
- [148] N. Keskar, R. Vijayalakshmi, M. Trivedi, K. Shenai, and P. Neudeck, "Characterization and Modeling of High-Voltage SiC P-i-N Diode," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1999, pp. 346-352.
- [149] M. Trivedi and K. Shenai, "Evaluation of Planar and Trench IGBT for Hard- and Soft-Switching Performance," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1999, pp. 717-721.
- [150] K. Chinnaswamy, P. Khandelwal, M. Trivedi, and K. Shenai, "Unclamped Inductive Switching Dynamics in Lateral and Vertical Power DMOSFETs," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1999, pp. 1085-1092.
- [151] N. Keskar, M. Trivedi, and K. Shenai, "Dynamic SOA of Power MOSFETs," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1999, pp. 1098-1102.
- [152] N. Keskar, M. Trivedi, and K. Shenai, "On the Reliability of DC-DC Power Converters," in *Proc. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1999, pp. 1639-1645.
- [153] S. Abedinpour, M. Trivedi, and K. Shenai, "One-Chip DC-DC Converter," in *Tech. Dig. Int. High Frequency Power Conversion (HFPC)*, 1999, pp. 144-151.
- [154] N. Keskar, M. Trivedi, and K. Shenai, "SOA Specifications for Increased Reliability," in *Tech. Dig. Int. High Frequency Power Conversion (HFPC)*, 1999, pp. 144-151.
- [155] S. Abedinpour, N. Keskar, M. Trivedi, and K. Shenai, "DC-DC Power Converter Development Using SiC Diode," in *Proc. PCIM Power Electronics Conf.*, 1999, pp. 189-195.
- [156] M. Trivedi and K. Shenai, "Data-Sheet Specification for Soft-Switching Application of IGBT," in *Proc. PCIM Power Electronics Conf.*, 1999, pp. 189-195.
- [157] M. Trivedi and K. Shenai, "Parasitic Extraction Methodology for Insulated Gate Bipolar Transistor," in *Proc. PCIM Power Electronics Conf.*, 1999, pp. 221-231.
- [158] R. Vijayalakshmi, M. Trivedi, and K. Shenai, "Impact of Switching Sequence on Zero Current Switching Performance of Power Bipolar Semiconductor Devices," in *Proc. IEEE Applied Power Electronics Conf. (APEC)*, 2000, pp. 1109-1114.
- [159] M. Trivedi and K. Shenai, "Parasitic Extraction Methodology for Insulated Gate Bipolar Transistor," in *Proc. IEEE Applied Power Electronics Conf. (APEC)*, 2000, pp. 1122-1128.
- [160] E. McShane and K. Shenai, "Correct-by-Design CAD Enhancement for EMI and Signal Integrity," in *Proc. IEEE Int. Symp. Quality Electronics Design (ISQED)*, 2000, pp. 341-345.
- [161] E. McShane, K. Shenai, and B. Blaes, "A Monolithic RF Microsystem in SOI CMOS for Low Power Operation in Radiation-Intense Environment," in *Proc. IEEE Aerospace Conf.*, 2000, pp. 421-429.
- [162] K. Shenai and M. Trivedi, "Silicon Carbide Power Electronics for High Temperature Applications," in *Proc. IEEE Aerospace Conf.*, 2000, pp. 431-437.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [163] E. McShane and K. Shenai, "Technologies and Designs of Low-Power RF Microsystem," in *Proc. IEEE Int. Conf. Microelectronics (MIEL)*, 2000, vol. 1, pp. 107-115.
- [164] M. Trivedi, V. John, T. Lipo, and K. Shenai, "Internal Dynamics of IGBT Under Fault Current Limiting Gate Control," in *Proc. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 2000, pp. 2903-2908.
- [165] S. Abedinpour, M. Trivedi, and K. Shenai, "DC-DC Power Converter for Monolithic Implementation," in *Proc. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 2000, pp. 2471-2475.
- [166] M. Trivedi and K. Shenai, "Performance of Silicon Carbide Devices in Power Converters," in *Proc. IEEE Int. Workshop Integrated Power Packaging (IWIPP)*, 2000, pp. 17-20.
- [167] E. McShane and K. Shenai, "Package Effects on Avalanche Rating of Power MOSFETs," in *Proc. IEEE Int. Workshop Integrated Power Packaging (IWIPP)*, 2000, pp.93-96.
- [168] E. McShane and K. Shenai, "RF De-Embedding Technique for Extracting Power MOSFET Package Parasitics," in *Proc. IEEE Int. Workshop Integrated Power Packaging (IWIPP)*, 2000, pp. 55-59.
- [169] E. McShane and K. Shenai, "A Curriculum in Radio Frequency ICs and VLSICs: Classroom Lessons and Laboratory Experiments from a Systems Perspective," in *Proc. IEEE Interdisciplinary Conf. Electrical, Electronics, and Computer Engineering Education (ICEECE)*, 2000.
- [170] E. McShane, M. Trivedi, and K. Shenai, "A Power Electronics Curriculum Oriented Toward Industry Applications: Classroom Lessons and Laboratory Experiments," in *Proc. IEEE Interdisciplinary Conf. Electrical, Electronics, and Computer Engineering Education (ICEECE)*, 2000.
- [171] S. Abedinpour and K. Shenai, "Power Electronics Technologies for the New Millennium," in *Proc IEEE Int. Caracas Conf. Devices, Circuits, and Systems (ICDCS)*, 2000, pp.P111/1-P111/9.
- [172] S. Abedinpour, R. Liu, G. Fasullo and K. Shenai, "Small-Signal Analysis of a New Asymmetrical Half-Bridge DC-DC Converter," in *Proc. IEEE Power Electronics Specialists Conf.(PESC)*, 2000, pp. 843-847.
- [173] A. Mulay and K. Shenai, "Performance Characterization of MOS and Bipolar Devices for the Development of Efficient and Reliable Electronics Ballast," in *Proc. IEEE Power Electronics Specialists Conf. (PESC)*, 2000, pp. 1600-1605.
- [174] K. Shenai and S. Abedinpour, "Semiconductor Technologies for High-Power Electronics in the New Millennium," in *Proc. Int. Sem. Power Semiconductors (ISPS)*, 2000, pp. 9-17.
- [175] E. McShane and K. Shenai, "Monolithic DC Power Supplies for Wireless Telecommunications and Multimedia Systems," in *Proc. IEEE Int. Telecommunications Energy Conf. (INTELEC)*, 2000, pp. 733-740.
- [176] E. McShane and K. Shenai, "Microwave Performance of Power MOSFETs on SOI Substrates," in *Proc. IEEE Cornell Conf.*, 2000, pp. 148-157.
- [177] M. Trivedi and K. Shenai, "High-Speed Switching Performance and Buck Converter Operation of 4H-SiC Diodes," in *Proc. IEEE Cornell Conf.*, 2000, pp. 69-78.
- [178] E. McShane and K. Shenai, "Circuit Modeling of RF Power MOSFETs including Package Parasitics," in *Proc. Int. Conf. Microelectronics and Packaging (SBMicro)*, 2000.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [179] M. Trivedi and K. Shenai, "Limitations Imposed by Package Parasitics on Soft-Switching Performance of IGBT," in *Proc. Int. Conf. Microelectronics and Packaging (SBMicro)*, 2000.
- [180] K. Shenai and M. Trivedi, "MOSFET Reliability Issues for Robust Power Converter Development," in *Proc. Int. Conf. Microelectronics and Packaging (SBMicro)*, 2000.
- [181] E. McShane and K. Shenai, "SOI Power MOSFETs for RF Wireless Communications," in *Proc. Int. Conf. Microelectronics and Packaging (SBMicro)*, 2000.
- [182] E. McShane and K. Shenai, "Monolithic Power Converter Technologies for Nanosatellite Constellations," in *Proc. Ann. Lunar Development Conf.*, 2000.
- [183] E. McShane and K. Shenai, "Mixed-Signal VLSI Enabling Technologies for Low-Power, Densely Integrated Spacecraft Avionics," in *Proc. Ann. Lunar Development Conf.*, 2000.
- [184] M. Trivedi, K. Shenai, and P. G. Neudeck, "Megawatt Power Electronics on Silicon Carbide for Space Applications," in *Proc. Ann. Lunar Development Conf.*, 2000.
- [185] M. Trivedi, K. Shenai and P. G. Neudeck, "Influence of Passivation Layer on High-Voltage Breakdown of SiC Mesa PiN Diodes" in *Proc. Electronic Materials Conf*, 2000.
- [186] K. Shenai, P. G. Neudeck, and G. Schwarze, "Design and Technology of Compact High-Power Converters," *Intersociety Energy Conversion Engineering Conf. (IECEC)*, 2000, pp. 30-36.
- [187] K. Shenai, and P. G. Neudeck, "Performance Evaluation of Silicon Carbide Devices in Power Converters," *Intersociety Energy Conversion Engineering Conf. (IECEC)*, 2000, pp.37-46.
- [188] K. Shenai, and P. J. Singh, S. Rao, D. Sorenson, K. Chu, and G. Gaylon, "On the Reliability of DC-DC Power Converters," *Intersociety Energy Conversion Engineering Conf. (IECEC)*, 2000, pp. 1480-1490.
- [189] K. Shenai, "New Millenium Ultra-Low Power Microsystems," in *Proc. National Aerospace Electronics Conf. (NAECON)*, 2000, pp. 459-468.
- [190] K. Shenai, "Silicon Carbide Power Converters for Next Generation Aerospace Electronics Application," in *Proc. National Aerospace Electronics Conf. (NAECON)*, 2000, pp.516-523.
- [191] K. Shenai, P. J. Singh, S. Rao, D. Sorenson, K. Chu, and G. Gaylon, "Power Supply Design for Performance and Reliability," in *Proc. National Aerospace Electronics Conf. (NAECON)*, 2000, pp. 524-531.
- [192] K. Shenai and P. G. Neudeck, "Performance of Silicon Carbide (SiC) JFETs in Power Converters," in *Proc. IEEE High Temperature Electronics Conf. (HiTEC)*, 2000.
- [193] M. Trivedi and K. Shenai, "Device Optimization and Modeling for Resonant Power Conversion," in *Proc. Int. Symp. Industrial Electronics (ISIE)*, 2000, pp. 370-373.
- [194] R. Vijayalakshmi, M. Trivedi, and K. Shenai, "Analytical Model for Power Bipolar Transistor in Hard- and Soft-Switching Applications," in *Proc. Int. Symp. Industrial Electronics (ISIE)*, 2000, pp. 374-378.
- [195] M. Trivedi, K-Shenai, and P. Joerg, "Evaluation of High-Voltage IGBT for Series Resonant DC-DC Converter Application," in *IEEE Appl. Power Elec. Conf. (APEC)*, 2001, pp. 1237-1241.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [196] K. Shenai and E. McShane, "Current Status and Emerging Trends in RF Power FET Technologies," in *IEEE Int. Microwave Symp. (IMS) Dig.*, Phoenix, AZ, 2001, pp. 1501-1504 (invited).
- [197] E. McShane, K. Shenai, and S. K. Leong, "A Silicon-on-Insulator 28-V RF Power LDMOSFET for 1-GHz Integrated Power Amplifier Applications," in *IEEE Int. Microwave Symp. (IMS) Dig.*, Phoenix, AZ, 2001, pp. 2135-2138.
- [198] M. Trivedi, K. Shenai, and P. G. Neudeck, "Characterization and Modeling of Low-voltage 4H-SiC Schottky and PN Diodes," in *Dig. Electronic Materials Conf.*, June 2001.
- [199] M. Trivedi and K. Shenai, "Hard- and Soft-Switching Buck Converter Performance of High-voltage 4H-SiC and Si P-i-N Diodes," *IEEE Ind. Appl. Soc. (IAS) Ann. Mtg.*, October 2001, pp. 391-395.
- [200] E. McShane and K. Shenai, "A CMOS Monolithic 5-MHz, 5-V, 250-mA, 56% Efficiency DC/DC Switch-Mode Boost Converter with Dynamic PWM for Embedded Power Management," *IEEE Industry Applications Society (IAS) Ann. Mtg.*, 2001, pp. 653-657.
- [201] E. McShane and K. Shenai, "Junction-to-Case Thermal Modeling and the Significance of the Junction Power Profile on Thermal Response," in *Dig. European Solid-State Device Res. Conf. (ESSDERC)*, 2001.
- [202] E. McShane and K. Shenai, "Thermal Robustness of Silicon-on-Insulator Versus Bulk Material in L-Band RF Power LDMOSFETs," in *Dig. European Solid-State Device Res. Conf. (ESSDERC)*, 2001.
- [203] S. Abedinpour, R. Burra, and K. Shenai, "Stress Analysis of a Full-Bridge ZVS DC-DC Converter," in *IEEE Ind. Appl. Soc. (IAS) Ann. Mtg. Digest*, October 2001, pp. 664-671.
- [204] S. Abedinpour, R. Burra, and K. Shenai, "Stress Two-Dimensional Finite Element Simulation and Stress Analysis of a Full-Bridge DC-DC Power Converter," in *IEEE INTELEC Dig.*, October 2001, pp. 205-212.
- [205] K. Shenai, "Power Semiconductor Devices: Design and Manufacturing for Improved Field Reliability," in *Proc. IEEE Int. Caracas Conf. Devices, Circuits, and Systems*, April 2002, pp. P024-1 – P024-2.
- [206] S. K. Mazumder and K. Shenai, "On the Reliability of Distributed Power Systems: A Macro to Micro Level Overview Using a Parallel DC-DC Converter," in *Dig. IEEE PESC*, 2002, vol. 2, pp. 809-814.
- [207] K. Shenai, "Semiconductor Technologies for Powering Micro Chips in the Information Age: From Source to Load," in *Dig. IEEE Int. Conf. Microelectronics (MIEL)*, 2002, vol. 1, pp. 3-6.
- [208] K. Acharya and K. Shenai, "On the  $dv/dt$  Rating of SiC Schottky Power Rectifiers," in *Proc. Power Electronics Technology Conference*, October 2002, pp. 672-677.
- [209] K. Shenai, C. Cavallaro, S. Musumeci and R. Pagano, "Modeling Low-Voltage Power MOSFETs as Synchronous Rectifiers in Buck Converter Applications," in *IEEE Ind. Appl. Soc. (IAS) Ann. Mtg. Digest*, October 2003, pp. 1794-1801.
- [210] C. Cavallaro, S. Musumeci, R. Pagano, A. Raciti and K. Shenai, "Analysis, Modeling and Simulation of Low-Voltage MOSFETs as Synchronous Rectifier Buck Converter Applications," in *IEEE IECON Dig.*, 2003, vol. 2, pp. 1697-1702.

**Silicon Valley Expert Witness Group, Inc.**  
**Consultant Curriculum Vitae**

- [211] Burra, R.K. Shenai, K., “CoolMOS Integral Diode: A Simple Analytical Reverse Recovery Model,” in *Dig. IEEE Power Electronics Specialist Conf. (PESC)*, vol. 2, pp. 834-838, June, 2003.
- [212] K. Shenai, “Power Management of Wireless OEM Devices,” in *Dig. IEEE Int. Conf. Microelectronics (MIEL)*, 2004, vol. 1, pp. 35-38 **(invited paper)**.
- [213] K. Shenai, “Power MOSFET Screening for Reliable Operation of DC-DC Power Converters,” in International Conference on Power Semiconductor Devices, Prague, Czech Republic, 2006 **(invited paper)**.
- [214] K. Shenai, “Advanced Electronic Systems Engineering,” in NanoUtah'06, The University of Utah, Salt Lake City, Utah, 2006 **(invited paper)**.
- [215] N. Jack and K. Shenai, “Magnetic Induction IC for Wireless Communication in RF-Impenetrable Media,” *IEEE Workshop on Microelectronics and Electron Devices (WMED)*, 2007, pp.47-48.
- [216] K. Shenai, N. Jack, “Sensing and Novel Underground Communication Technology for Soil and Water Management,” Abstract Accepted, *The Second International Symposium on Soil Water Measurement using Capacitance, Impedance, and Time Domain Transmission*, Beltsville, Maryland, 2007.
- [217] K. Shenai, “Field-Reliability of an Automotive Switch— a New Paradigm,” Abstract Accepted, *Twelfth Annual Automotive Electronics Reliability Workshop*, Nashville, TN, May 2007.
- [218] K. Shenai, “A ”Good” Automotive Power MOSFET Switch,” Abstract Accepted, *Twelfth Annual Automotive Electronics Reliability Workshop*, Nashville, TN, May 2007.
- [219] S. B. Jones and K. Shenai, “Subsurface measurement needs for ecological, hydrological and agricultural applications,” *IEEE Midwest Symposium on Circuits and Systems (MWSCAS)*, 2007, pp. 754-757.
- [220] S. Sen, A. Sokolow, R. P. Simion, D. Sun, R. L. Doney, M. Nakagawa, J. H. Agui, Jr. and K. Shenai, “Ocean waves, mechanical impulses and electrical energy: concept of a simple conversion process,” *International Conference on Advances in Energy Research, 2007*, pp 329-334.
- [221] L. E. Gilcrist, G. S. Baker, S. Swaminathan, D. P. Visco, R. Bharadwaj, S. Mukhopadhyay, K. Shenai and S. Sen, “Acoustic interrogation of soil and possible remote detection of shallow buried inclusions,” *IEEE Northeast Workshop on Circuits and Systems (NEWCAS)*, 2007, pp. 758-761.
- [222] K. Shenai, “Cognitive Power Grid – an Intelligent Electric Energy Management System to Fuel Global Information Economy,” in *Digest of IEEE Electrical Power Conference 2007*, October 25-26, 2007, Montreal, Quebec, Canada **(invited Keynote Paper)**
- [223] R. Bharadwaj, S. Mukhopadhyay, M. Peralta, K. Shenai and S. Majumder,” Cognitive Distributed Networks in Environmental e-Science,” *Proc. IEEE International Workshop on Future Trends of Distributed Computing Systems (FTDCS)*, 2008, pp. 192-198.
- [224] K. Shenai and S. Mukhopadhyay, “Cognitive Sensor Networks,” in *Dig. IEEE Int. Conf. Microelectronics (MIEL)*, pp. 315-320, May 11-14, 2008 **(invited paper)**.

## **Silicon Valley Expert Witness Group, Inc. Consultant Curriculum Vitae**

- [225] R. Bharadwaj, S. Mukhopadhyay, M. Peralta, K. Shenai, and S. Majumder, "Cognitive Distributed Networks in Environmental e-Science," in *Digest of 12<sup>th</sup> IEEE Int. Workshop on Future Trends of Distributed Computing Systems*, pp. 192-196, October 21-23, 2008, Kunming, China.
- [226] K. Shenai, "Grand Challenges in Power Semiconductors," in *Proc. IEEE Int. Conf. Electron Devices and Solid-State Circuits*, December 8-10, 2008, pp. 1-4 (**invited paper**).
- [227] K. Shenai, "Smart Sensing and Monitoring of Ecosystem Dynamics," in *Digest of EnviroEnergy2009*, March 19-22, 2009, Chandigarh, India (**invited Plenary Paper**).
- [228] P. Boyapati and K. Shenai, "Wireless Soil Moisture Sensor," in *Digest of EnviroEnergy2009*, March 19-22, 2009, Chandigarh, India.
- [229] P. Boyapati and K. Shenai, "Wireless Soil Electrical Conductivity Sensor," in *Digest of EnviroEnergy2009*, March 19-22, 2009, Chandigarh, India.
- [230] K. Shenai, "Beyond Silicon ...," Plenary Paper to be presented at the *Int. Workshop on Physics of Semiconductor Devices (IWPSD)*, December 2009, New Delhi, India (**invited**).

### **Professional Associations and Achievements**

- Fellow, IEEE
- Fellow, AAAS
- Fellow, Institution of Electrical and Telecommunication Engineers (IETE), India
- Member, Yugoslavian National Academy of Engineering, Belgrade, Yugoslavia
- First Utah Science, Technology, and Research (USTAR) Endowed Professor on *Intelligent Systems* (2005-2007)
- Member, New York Academy of Sciences
- Listed in *Who's Who in Technology* and *Who's Who in Engineering*
- Distinguished Lecturer, IEEE Electron Devices Society (1995-)
- Co-author of a Best Student Paper Award, 1994 IEEE BCTM
- Elected Member, IEEE Electron Device Society AdCom (1998-2000, 2001-2003)
- Society Representative of IEEE Electron Devices Society to IEEE Intelligent Systems Council (2002-2004).
- University Scholar Award for Outstanding Research and Teaching, University of Illinois (1998-2001)
- William Brown Award, Space Studies Institute, Princeton, NJ (1998)
- Foundation for Non-Military Development of Space (FINDS) Award (1998)
- IEEE Chapter Award, Yugoslavia (2000)
- Faculty Research Excellence Award, College of Engineering, The University of Illinois at Chicago (2000)
- Distinguished Professor, University of Nis, Nis, Yugoslavia (2000)

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## Consultant Curriculum Vitae

### Professional Society Administration

- Elected Member, IEEE Electron Devices Society AdCom (1998-2000).
- Elected Member, IEEE Electron Devices Society AdCom (2001-2003).
- Society Representative of IEEE Electron Devices Society to IEEE Intelligent Systems Council (2002-2004).

### Professional Society Chapter Activities

- Vice Chairman, IEEE MTT Chapter, Schenectady, NY (1989-1990).
- Founding Chairman, IEEE EDS/MTT/LEOS Chapter, Oregon Section, Portland, OR (1991-1994).
- Member, IEEE Electron Device Society (EDS) Chapter Committee, 1998-2002.

### Professional Society Technical Committee Activities

- Member, *Standards Committee*, IEEE Power Electronics Society, 1997-2002.
- Member, *Packaging Committee*, IEEE Power Electronics Society (PELS) – IEEE Industry Applications Society (IAS) -- Power Sources Manufacturers Association (PSMA), 1997 - 2002.
- Member, *Model Validation Committee*, IEEE Power Electronics Society (PELS) - IEEE Industry Applications Society (IAS), 1996-2002.
- Member, *Power Semiconductor Devices*, IEEE Electron Devices Society (EDS), 1998-2002.
- Member, *Modeling Committee*, IEEE Electron Devices Society (EDS), 2000-2002.

### Professional Panel Activities

- Member, NSF SBIR Panel on Solid-State and Microstructure Sciences, 1990.
- Organizer and Moderator, "Power Semiconductors: A User's Perspective," *Third IEEE Int. Symp. Power Semiconductor Devices and IC's (ISPSD)*, Baltimore, MD, 1991.
- Organizer and Moderator, "Frontiers in Silicon Devices for the 1990's," *IEEE Device Research Conference (DRC)*, Boulder, CO, June 1991.
- Organizer and Moderator, "Frontiers for Indo-US Collaboration in Optoelectronics," *First IEEE Int. Conf. Emerging Optoelectronic Technologies (CEOT)*, Bangalore, India, December 1991.
- Member, US NSF SBIR Panel on Solid-State and Microstructure Sciences, 1994.
- Member, "What is Design Quality? How can Quality in Electronic Design be Quantified?" Organized by: M. Reinhardt, Rubicad, Moderated by: M. Santarini, EE Times, in *Proc. IEEE Int. Symp. Quality of Electronic Design (ISQED)*, March 21, 1998.

## Silicon Valley Expert Witness Group, Inc. Consultant Curriculum Vitae

### ▪ Professional Short Courses

- Organizer and Principal Lecturer, “Power Electronics: Components & Systems,” UC Berkeley, 1990. Other lecturers included C. A. T. Salama, B. J. Baliga, W. McMurray and R. D. Middlebrook.
- Lecturer, “Power Semiconductor Devices & High-Voltage IC's,” *IEEE International Symp. Power Semiconductor Devices and IC's*, Baltimore, MD, 1991. Other lecturers included C. A. T. Salama, B. J. Baliga, and A. Shibib.
- Organizer and Lecturer, “VLSI Circuit Processing,” *SPIE/IEEE Conf. Emerging Optoelectronics Technologies (CEOT)*, Bangalore, India, December 1991.
- Organizer and Lecturer, “Advanced BiCMOS ULSI Technologies,” *SPIE Microelectronics Symposium*, San Jose, CA, 1992.
- D. Divan, K. Shenai, R. Lorenz, T. Lipo and R. Schneider (instructors) *Power Electronics: Circuits, Systems, and Industrial Applications*, November 1-3, 1993; November 7-9, 1994; and May 1-4, 1995.
- K. Shenai, “Applications of SABER in Research and Teaching Programs at the University of Wisconsin - Madison,” *SABER: Bringing Universities and Industry Together*, Livonia, MI, September 8, 1994.
- K. Shenai, “Power Semiconductor Devices: Technologies and Applications,” Departamento de Engenharia Electronica, Escola de Engenharia da UFMG, Belo Horizonte - M.G., Brazil, Aug. 6 - 12, 1995.
- K. Shenai (Organizer and Principal Instructor) and G. Estep, “Low-power RF IC Design,” University of Illinois at Chicago, Chicago, IL, October 21-23, 1996.
- K. Shenai, “Power semiconductor device and circuit interactions,” in 2-day Workshop on Integrated Power, PCIM, Las Vegas, September, 1996. Workshop organized by J. Fishbein, Burgquist Co., Minneapolis, MN.
- K. Shenai, “Application-Specific Power Electronics,” Department of Electronics, Government of India, New Delhi, India, December 31, 1996.
- K. Shenai, “Power MOSFETs,” Littlefuse Inc., Warrenville, IL (1998).
- Organizer and Lecturer, “Power Semiconductor Design,” IEEE APEC, Dallas, TX, 1999.

### ▪ Journal Editorship

- Regional Editor, *Int. J. Circuits, Systems and Computers (JCSC)* (2008 - present).
- Editor, *IEEE Trans. Electron Devices* (1990-2002).
- Editor-in-Chief, *IEEE Electron Devices Society Newsletter* (1995-2002).
- Associate Editor, *Int. J. Circuits, Systems and Computers* (1996-2000).
- Guest Editor, Special Issue of *J. IETE, India* (invited) on “Submicron Metallization Technologies,” March 1991 (**invited**).
- Guest Editor, Special Issue of *IEEE J. Solid-State Circuits* (invited) on “High-Speed IC Design,” October 1994 (**invited**).
- Guest Editor, Special Issue of *IEEE Trans. Electron Devices* (invited) on “Submicron Bipolar/BiCMOS Devices and Technologies,” March 1995 (**invited**).

## **Silicon Valley Expert Witness Group, Inc.** **Consultant Curriculum Vitae**

- Guest Editor, Special Issue of *IEEE J. Solid-State Circuits* (invited) on “High-Speed IC Design,” January 1996 (**invited**).

### **Conference Organization**

- Founder and Organizer, *First IEEE Int. Conf. Emerging Optoelectronic Technologies (CEOT)*, Bangalore, India, December 1991.
- Organizer, *SPIE Symp. Submicron Metallization*, San Jose, CA, 1992.
- Organizer, *First Workshop on Custom Design of Application-Specific Power Semiconductor Devices and Circuits*, Madison, WI, April 13-14, 1994.
- Organizer, *Second Int. IEEE/SPIE Conf. Emerging Optoelectronics Technologies (CEOT)*, Bangalore, India, July 18-21, 1994.
- Founder and Organizer, *IEEE Int. Workshop on Integrated Power Packaging (IWIPP)*, Chicago, IL, April 1998.

### **Conference Management**

- Chairman, *First IEEE Int. Conf. Emerging Optoelectronic Technologies (CEOT)*, Bangalore, India, December 1991.
- Chairman, *SPIE Symp. Submicron Metallization*, San Jose, CA, 1992.
- Chairman, Process Technology Subcommittee, *IEEE Bipolar/BiCMOS Circuits and Technologies (BCTM)*, Minneapolis, MN, October 1993.
- Co-Chairman, *First Workshop on Custom Design of Application-Specific Power Semiconductor Devices and Circuits*, Madison, WI, April 13-14, 1994.
- Co-Chairman, *Second Int. IEEE/SPIE Conf. Emerging Optoelectronic Technologies (CEOT)*, Bangalore, India, July 18-21, 1994.
- Vice Chairman, Technical Program Committee, *IEEE Bipolar/BiCMOS Circuits and Technologies (BCTM)*, Minneapolis, MN, October, 1994.
- Chairman, Poster Sessions, *1994 IEEE Int. Integrated Reliability Workshop (IRW)*, Lake Tahoe, CA, October 16-19, 1994.
- Vice Chairman, Process/Device Subcommittee, *1995 IEEE Int. Reliability Physics Symposium (IRPS)*, Las Vegas, NV, April 3-6, 1995.
- Chairman, Technical Program Committee, *IEEE Bipolar/BiCMOS Circuits and Technologies (BCTM)*, Minneapolis, MN, October 1995.
- Chairman, Finance Committee, *International IEEE Conference on Power Electronics, Drives and Electrical Systems*, New Delhi, India, January 1996.
- General Chairman, *IEEE Bipolar/BiCMOS Circuits and Technologies (BCTM)*, Minneapolis, MN, October 1996.
- Chairman, Exhibitions and Vendor Show, *IEEE Bipolar/BiCMOS Circuits and Technologies (BCTM)*, Minneapolis, MN, October 1997.
- Vice Chairman, *Int. Conf. Microelectronics (MIEL)*, Nis, Yugoslavia, September 15-17, 1997.
- General Chairman, *IEEE Int. Workshop on Integrated Power Packaging (IWIPP)*, Chicago, IL, April 1998.

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- Vice Chairman, *Int. Conf. Microelectronics (MIEL)*, Nis, Yugoslavia, 1999.
- General Chairman, *IEEE Int. Workshop on Integrated Power Packaging (IWIPP)*, 2000.
- Organizer and Chairman, Special Session on Recent Advances in Power Electronics, *IEEE Antennas and Propagation Society, URSI B and D Int. Symp.*, Boulder, CO, 2001.
- Vice Chairman, *Int. Conf. Microelectronics (MIEL)*, Nis, Yugoslavia, 2002.
- Vice Chairman, *Int. Conf. Microelectronics (MIEL)*, Nis, Yugoslavia, 2004.
- Vice Chairman, *Int. Conf. Microelectronics (MIEL)*, Nis, Yugoslavia, 2006.

### **Conference Committee Membership**

- *High-Frequency Power Conversion Conference*, Intertec Communications, Ventura, CA, 1989.
- *Workshop on Tungsten and Other Advanced Metals for ULSI*, Materials Research Society (MRS) and the University of California, Berkeley, CA (1989-1991).
- *IEEE/SPIE Conference on Advances in Packaging*, Boston, MA, 1990.
- Solid State Devices Subcommittee, *IEEE International Electron Devices Meeting (IEDM)* (1990-1991).
- *IEEE Device Research Conference (DRC)*, Boulder, CO, June 1991.
- *Third IEEE Int. Symp. Power Semiconductor Devices and IC's (ISPSD)*, Baltimore, MD, 1991.
- International Advisory Committee, *Int. Symp. Semiconductor Modeling & Simulation*, March 1993.
- Process/Device Subcommittee, *IEEE Int. Reliability Physics Symposium (IRPS)*, San Jose, CA, April 11-14, 1994.
- International Steering Committee, *1995 International Power Electronic Conference (IPEC)*, Yokohama, Japan, April 3-7, 1995.
- International Steering Committee, *International IEEE Conference on Power Electronics and Drive Systems (PEDS'95)*, Singapore, February 21-24, 1995.
- Power Device Sub Committee, *IEEE Applied Power Electronics Conf. and Exposition (APEC)*, February 23-27, 1997, Atlanta, GA.
- *Int. Conf. Power Semiconductor Devices*, Prague, Czech Republic, 1999.
- *Int. Conf. Power Semiconductor Devices*, Prague, Czech Republic, 2001.
- *Int. Conf. Power Semiconductor Devices*, Prague, Czech Republic, 2003.
- *Int. Conf. Power Semiconductor Devices*, Prague, Czech Republic, 2005.
- International Advisory Committee, *Int. Conf. Microelectronics (MIEL)*, Nis, Yugoslavia, 2008.
- International Advisory Committee, *2008 IEEE Int. Conf. Electron Devices and Solid-State Circuits*, December 8-10, 2008, Hong Kong, China.
- International Advisory Committee, *Int. Conf. Microelectronics (MIEL)*, Nis, Yugoslavia, 2010.

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